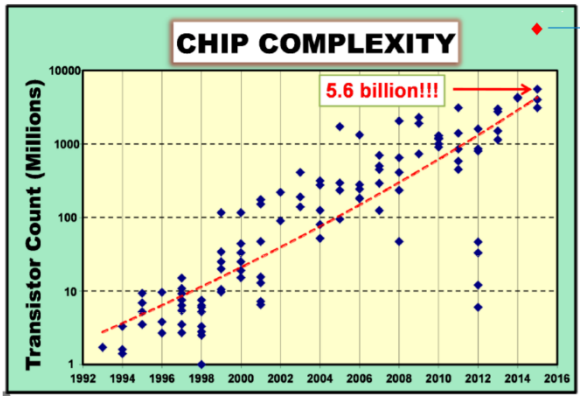


New York University Tandon School of Engineering

Electrical and Computer Engineering

Course Outline ECE 6443 [VLSI System and Architecture Design], Fall 2019

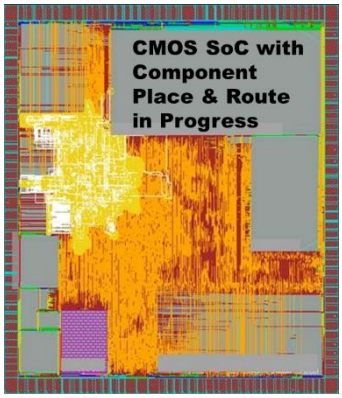
Instructor: Azeez Bhavnagarwala

To contact instructor: **ajb20@nyu.edu**

Class Lecture: **Thursdays 6:00 PM – 8:30 PM**

Office hours: **Thursdays 2 PM-4 PM** (Room: 817, 370 Jay Street) or by appointment,

Course Pre-requisites: Basic knowledge of Semiconductor Device Physics, CMOS Digital Circuit Design and Computer Organization is assumed. Please see instructor if you do not have any of these. If you have not taken ECE 6473 (or an equivalent) you must take ECE 6473 concurrently.



Summary Course Description: ECE 6443 introduces students to Design Automation and functional verification of digital semiconductor components with industry-typical code, tools and flows to enable delivery of semiconductor CMOS System-on-Chip (SoC) products to customers *sooner* and at *lower cost* despite their *increasing complexity* and *scale*, and despite their *increasing capability, performance* and *energy efficiency* over the last 30 years.

The class begins with an introduction to Verilog followed by its use in developing designs of digital components across a broad range of applications – combinational logic, arithmetic functions, memory elements, state machines etc. We will review design guidelines (and verification simulations) for combinational and sequential circuits and in detail the design of components of an ALU, an FSM and of single and multi-port memory arrays.

RTL Verilog code, design constraints and standard cell libraries are applied as inputs to Synthesis tools that generate a gate level netlist as its output. With design constraints on timing, we will iteratively synthesize the schematic of the designs we developed using Synthesis tools until timing constraints can be met. We meet these requirements by using a Static Timing Analysis which propagates Actual Arrival Times and Required Arrival Times to the pins of every gate or cell in the design that are responsible for timing failures.

When attempting to automate the place and route of synthesized circuits with physical design tools, we will review common strategies and algorithms to partition blocks into smaller modules while floor-planning, to mitigate the impact of their design complexity on wire routability/delays and the timing violations they produce. We complete the path from RTL to GDS by reviewing power delivery planning and clock tree synthesis.

Course Content Schedule: Weekly lecture slide sets & lab assignments, to be generally available on NYU classes at the start of each work week. Assignments are due weekly on the following Thursday by 5 PM. Please submit lab assignments as PDFs or Word documents with your identifying information and not on hand-written sheets of paper. Please include your analysis and justify each of your design choices. Include Verilog code, Simulation results & waveforms. Please prefix your lab assignment submission file name with your netID followed by the assignment number. For example, I would submit Lab Assignment 4 as a PDF document with filename: *ajb20_Lab4.pdf*

Course structure:

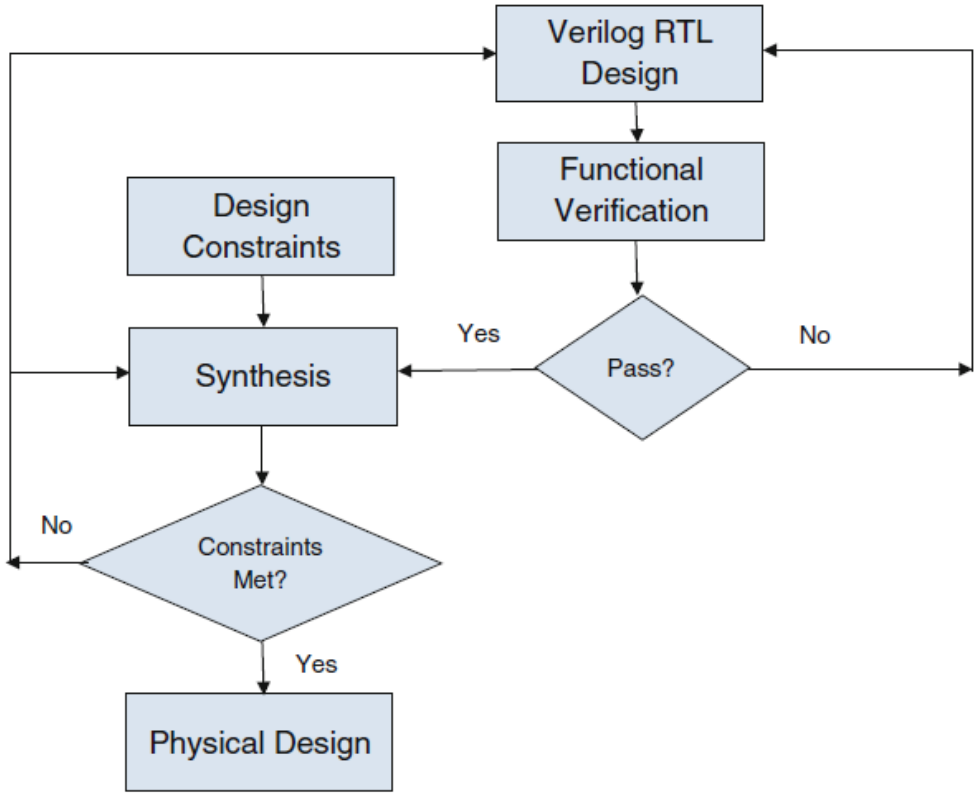
Your performance in the course will be assessed with **weekly assignments** (30% of total grade - that include a circuit design and simulation lab using ModelSim from Mentor Graphics with design problems), a **midterm** (30% of total grade), Group Project (10% of grade) and a **final** (30% of total grade). In addition, there will be (ungraded/extra-credit) pop-quizzes - Participation in these activities is highly encouraged.

Course Textbooks: [1] S Ramachandran VLSI, [2] A Kahng, VLSI Physical Design, [3] J Bhaskar, Static Timing Analysis (PDF of all of these are uploaded to NYU Classes)

Course Schedule:

Week	Date	ECE 6443 Content	LAB
1	*9/2 – 9/8*	***Design automation and its impact on sustaining Moore's Law***. Levels of design abstraction in digital design. Structural, behavioral and *Synthesizable RTL* descriptions using ***Verilog:*** Verilog operators. Synthesized logic gates, Synthesizable RTL for arithmetic & logic circuits – multi-bit adders, subtractors, comparators, decoders, multiplexors, parity detectors, code convertors, priority encoders & barrel shifters.	Lab 1
2	*9/9 – 9/15*	***Combinational logic code structures*** – use of blocking assignments & event queue, continuous/procedural assignments, incomplete sensitivity lists, combinational loops, unintentional latches, if-else Vs Case statements, priority structures, Logical/Case equality and inequality operators, arithmetic resource sharing, multiple driver assignments.	Lab 2
3	*9/16 – 9/22*	***Sequential circuit block Verilog descriptions*** – positive and negative level sensitive D Latch, edge-triggered D Flip-Flops, Flip-Flops with synchronous load and synchronous reset. Synchronous counters, timing and performance evaluation of sequential circuits. Blocking, Non-Blocking assignments and 'always' blocks. Latch Vs Flip-Flop as Level Vs Edge triggered components, use of Synchronous Vs Asynchronous Reset, If-Else Vs Case, Gated clocks and use of pipelining in design, Multiple clock domains, multi-phase clocks.	Lab 3
4	*9/23 – 9/29*	***Complex Designs in Verilog***: ALU design, Module to count 1's, Parity generator and detectors, Parity checker, Finite State Machines: Moore Vs Mealy, Toggle Flip-Flop and Level to pulse conversion, FSM encoding: Binary, Gray, One-Hot Encoding, sequence detectors using FSM, more example uses of FSM as BIST engines to test SRAM at speed. ASIC Design flow, synthesis and optimization techniques.	Lab 4
5	*9/30 – 10/6*	***Static Timing Analysis*** – complete, exhaustive method of verifying timing of the entire design. Design Constraints on timing, Clock, skew, input & output delay. Timing arcs and unateness, Min & Max timing paths, operating conditions. ***Standard Cell Library and timing models*** for combinational and sequential cells. Synchronous checks – setup and hold checks, negative values in setup and hold checks, recovery and removal checks, pulse width checks, State-dependent models, Interface timing models, Models for cross-talk noise analysis, 2-stage cells and for multistage and sequential cells. Standard cell library power dissipation models – active, leakage power, double counting of clock pin power and other attributes of standard cell library. ***Representation of interconnect parasitics*** – wireload models, interconnect trees, extracted parasitics, representing coupling capacitances, hierarchical methodology, reducing parasitics in critical nets – reducing wire resistance and increasing wire spacing	Lab 5
6	*10/7 – 10/13*	***Delay calculations***, Elmore delay, higher order interconnect delay estimation, full-chip delay calculation. Flip-Flop path delays, Cross-talk & noise, glitch threshold and propagation, aggressor timing correlation, ***Timing verification***, multicycle paths, false paths, half-cycle paths, timing across clock domains – slow to fast and fast to slow, On-chip variations, OCV for hold-checks, *Back-annotation formats*: SPEF and SDF, Sign-off methodology – PVT corners, Parasitic Interconnect corners, operating modes, multi-mode/corner analysis. ***Statistical Static Timing Analysis*** – process & interconnect variations, Statistical Timing Libraries. *Failed Timing paths*, large I/O delays, half-cycle paths, large transition times, missing multi-cycle hold	Lab 6

Week	Date	ECE 6443 Content	LAB
7	*10/28 – 11/3*	Constraints on ***Physical Design automation*** algorithms – Technology (min geometry/spacing), Electrical (timing constraints on signal delay/integrity) and Methodology (routing/min wirelength). Placement and routing algorithms and complexity, algorithm types and quality, graphs theory, Rent's Rule: Netlist and system partitioning to minimize complexity and IO, pin and net oriented netlists	Lab 7
8	*11/4 – 11/10*	The ***Group Project*** requires students to use commercial tools [VCS, Verdi, Design Compiler, PrimeTime, IC Compiler] to design and build an SRAM BIST engine. These tools enable implementation of an industry-typical design flow from RTL to GDS for a foundational IP block that uses combinational and sequential circuit components. The BIST FSM asserts simple test patterns (blanket 0, blanket 1, checkerboard) to verify functionality of SRAM arrays at speed. ***Teams of 4 students*** design the BIST in Verilog, synthesize a netlist of the BIST component hierarchy, verify functionality with gate level netlist simulations, impose modest timing constraints, perform static timing analysis that includes identifying timing failure nodes, types and design fixes to meet timing closure. (if time and tool functionality permit: perform static timing analysis on gate level netlists of design after place & route of physical design using standard cell library components)	Group Project
9	*11/11 – 11/17*		
10	*11/18 – 11/24*		
11	*11/25 – 12/1*		
12	*12/2 – 12/13*	*Review for Final*	**Final Exam 12/19**



Simulation and synthesis flow

Policy on Academic Honesty:

In pursuing these goals, NYU expects and requires its students to adhere to the highest standards of scholarship, research and academic conduct. Essential to the process of teaching and learning is the periodic assessment of students' academic progress through measures such as papers, examinations, presentations, and other projects. Academic dishonesty compromises the validity of these assessments as well as the relationship of trust within the community. Students who engage in such behavior will be subject to review and the possible imposition of penalties in accordance with the standards, practices, and procedures of NYU and its colleges and schools. Violations may result in failure on a particular assignment, failure in a course, suspension or expulsion from the University, or other penalties.

More details about specific actions that constitute a violation of the NYU policy can be found here.

https://www.nyu.edu/about/policies-guidelines-compliance/policies-and-guidelines/academic-integrity-for-students-at-nyu.html.

Moses Center Statement of Disability:

If you are student with a disability who is requesting accommodations, please contact New York University's Moses Center for Students with Disabilities at 212-998-4980 or mosescsd@nyu.edu. You must be registered with CSD to receive accommodations. Information about the Moses Center can be found at www.nyu.edu/csd. The Moses Center is located at 726 Broadway on the 2nd floor.