**ECE-GY-6463- Course outline**

**Instructor: Ramesh Karri (rkarri@nyu.edu, cell: 917 363 9703, office hours TBD; office: TBD**

Field Programmable Gate Arrays (FPGAs) are used in telecommunication, video processing, cryptography, control and biomedical applications. This course will provide an understanding of FPGA-based design starting from a VHDL (An industry standard) hardware description language specification of a design. One will learn how to model, simulate, and synthesize digital logic using a hardware description language (VHDL). Initially you will model simple digital logic building blocks (AND, OR, XOR, Multiplexer, Demultiplexer, Flip Flop etc). You will then model larger digital logic building blocks (Rotate by a fixed amount, Data dependent rotate, add and subtract). You will then model controllers. Finally, you will compose the building blocks into a large digital logic data path + controller that will then be implemented on an FPGA. The course is structured as a combination of lectures and labs. By the end of the course, students should be able to: (1) Design a complex digital system using VHDL modeling and synthesis language (2) Implement, verify, and test a digital system in FPGA hardware.

**Week-by-week lecture schedule (tentative)**

1. Intro to VHDL and FPGA Design I– Model digital logic building blocks using VHDL (AND, OR, XOR, Multiplexer, Demultiplexer, Flip Flop, rotate input by a fixed amount, data dependent rotate, add, subtract etc). Installing simulation (Modelsim), synthesis tools (Xilinx) and order development board. (1-2 Weeks)
2. Introduction to VHDL and FPGA design II - Check that these models are functionally correct (Functional Simulation) and correct from a timing perspective (Timing simulation) using Modelsim simulator. Map and download the design onto an FPGA and verify the function (Perform synthesis, place and route). (2 Weeks)
3. Real Life Application I - Model RC5 Encryption (with fixed round keys) in Hardware. Perform Functional and Timing simulation. (2 Weeks)
4. Real Life Application II – Model RC5 Round Key Generation application and perform Functional and Timing Simulation. (2 Weeks); controller modeling
5. Structural Modeling – Understand how to structurally connect components. Connect RC5 Encryption with Round key generation to create a complete RC5 Encryption Design. Assign course Projects (1 Week)
6. FPGA Development Board - Understand the FPGA development board; Learn how to target a design onto the FPGA development board using placement constraints; download entire RC5 Encryption design onto the FPGA development board and observe correct functionality. (2 Weeks)
7. Testbenches – Automated, self checking Testbenches in VHDL for design verification (2 Weeks)
8. Electronic Systems Level Synthesis (c-based design)
9. Final Project Presentations/Demoes (1 week)

Lab 1- Implement leftrotate and rightrotate in VHDL; perform functional and timing simulation. (due week 2).
Lab 2- Implement partial RC5 Encryption and Decryption function. (due week 3)
Lab 3- Implement complete RC5 Encryption and Decryption function with fixed round keys. (due week 4)
Lab 4– Structural Modeling – Put together Key Expansion, Encryption, and Decryption modules to implement the complete RC5 Encryption/Decryption Chip. (due week 6)
Lab 5– Testbench Design – an automated testbench for the RC5 Encryption/Decryption design. (due week 8)
Lab 6 – Use FPGA Development Board – Demo RC5 Encryption on the FPGA development board. Detailed documentation including diagrams etc (due week 9).
NEW !!: Labs 7.

**Final Project**: One example: Implement an 8-bit processor on an FPGA. Implement at least 10 instructions. The final report will include an: 1. Overview of the processor. 2. Functional Simulation of the processor; 3 Timing Simulation of the processor, 4. Testbench; 5. Demonstration of functionality on the FPGA (run a simple program on the processor.); Due week 14 before start of the class.
***NO Textbook: Buy a Xilinx FPGA Board in lieu of textbook (mandatory). Course notes.***

**REFERENCE Text Books:** If you want to buy a textbook for this course you can get` 1. "VHDL Programming by Example" by Douglas L. Perry ISBN 007140070-2. Or 2. VHDL a starters guide by Sudhakar Yalamanchili.
**Grading:** Quizzes: 10% (at the beginning of every lecture); Exam 1: 25% (mid term-Lecture 8 in class on October 27); Exam 2: 25% (final; During finals week; scheduled by the registrar); Class project: 20% ; Labs: 25%