New York University Tandon School of Engineering

Electrical and Computer Engineering

Course Outline ECE 6473 [Introduction to VLSI Design], Fall 2019

Instructor: Azeez Bhavnagarwala

To contact instructor: **ajb20@nyu.edu**

Class Lecture: **Mondays 9:50 AM – 12:20 PM**

Office hours: **Monday 2PM-4PM** (Room: 817, 370 Jay Street) or by appointment,

Course Pre-requisites: Basic knowledge of Semiconductor Device Physics, Digital Design and Computer Organization is assumed. Please see instructor if you do not have any of these.

Summary Course Description: ECE 6473 details the electrical design of digital CMOS circuits and techniques across a wide range of System-on-Chip (SoC) semiconductor components. Focus of the course is on imbuing best-in-class circuit design practices by industry with weekly circuit design labs using EDA tools and advanced CMOS FinFET technology parameter decks. The course advances from the study of basic CMOS logic and memory circuit building blocks to complex components ranging from clock tree networks, large dimension (256x256) matrix multipliers, dense (>150 Mb) GPU Register File circuits and Content Addressable Memories in networking ASICs. If the schedule permits, we will also look at recent trends in processing-in-memory circuits and processing near memory components in compute limited hardware accelerators.

Course Content Schedule: Weekly lecture slide sets, lab assignments, IEEE reading assignments to be generally available on NYU classes at the start of the week. Assignments are due weekly on the following Monday by 5 PM. Please submit lab assignments as PDFs or Word documents with your identifying information and not on hand-written sheets of paper. Please include your analysis and justifications for your design choices with your circuit simulations/waveforms. Please prefix your lab assignment submission file name with your netID followed by the assignment number. For example, I would submit Lab Assignment 4 as a PDF document with filename:*ajb20_Lab4.pdf*

Course structure:

Your performance in the course will be assessed with your performance in **weekly assignments** (30% of total grade), that include a circuit design and simulation lab, circuit design problems and a review of a relevant assigned IEEE publication, a **midterm** (30% of total grade) and a **final** (40% of total grade). In addition, there will be (ungraded/extra-credit) pop-quizzes, Participation in these activities is highly encouraged.

Course Textbooks:

[1] Neil Weste and David Harris, "CMOS VLSI Design" [3rd or later Edition], Addison-Wesley.

[2] J. Uyemura, "Introduction to VLSI Circuits and Systems", Wiley, 2002.

[3] J Rabaey, A Chandrakasan, B Nikolic, "Digital Integrated Circuits" 2nd Edition, Prentice Hall, 2003

Course Schedule:

Week	Date	ECE 6473 Content	Assignments
1	*9/3 – 9/9*	Introduction to electrical design of digital CMOS circuit components, Lab setup and access to Cadence Virtuoso EDA tools for Schematic entry and HSPICE based circuit simulation using PTM BSIM models for advanced CMOS FinFET technologies (16nm/10nm/7nm)	Lab 1
2	*9/10 – 9/16*	MOSFET device physics, Drain current models across all regions of operation, short channel behavior, Planar and FinFET device structures, physical limits on scaling transistor geometries and operating voltages. Device capacitances, device leakage current components and electrical uncertainty of device behavior. Basic (planar) CMOS process integration and manufacturing	Lab 2
3	*9/17 – 9/23*	Electrical models of on-chip wiring with R, C & L parameters. Delay models for wire-tree networks, Elmore's model, ideal, lumped, & distributed wire models, transmission line models. Wire limited chip and package design.	Lab 3
4	*9/24 – 9/30*	Electrical design of basic CMOS circuit building blocks with a detailed analysis of an inverter extended to combinational logic gates and design styles in CMOS including Static CMOS logic & Dynamic CMOS circuits. Circuit design techniques for speed, energy efficiency, area efficiency and electrical robustness to uncertainty from noise, manufacturing variations random variations, and variations in temperature and operating voltage.	Lab 4
5	*10/1 – 10/7*	Design and analysis of sequential circuits – basic components of CMOS static latches, Flip-flops. Master-slave edge triggered flip-flops, true single-phase clocked latches, pulsed flip-flops, setup and hold time definitions, hold time violations and their fixes.	Lab 5
6	*10/8 – 10/14*	Interconnect limitations on chip performance, signal integrity, energy efficiency and BEOL chip manufacturing costs. Cross-talk, voltage droop from power distribution, wire delay scaling. Inductance and performance limitations of Transmission Line effects	Lab 6
Monday October 21st		**Midterm Test**	
7	*10/29 – 11/4*	Synchronous Design: Timing basics, Clock distribution techniques, sources of clock skew and jitter, Self-timed logic – an asynchronous technique, Clock synthesis and synchronization using a Phase Locked Loop, Distributed Clocking using DLL, Synchronous Vs Asynchronous designs	Lab 7
8	*11/5 – 11/11*	Arithmetic building blocks, the Datapath in processors, Full Adder, Multipliers, partial product generation, accumulation, final addition, Barrell shifters, logarithmic shifter. Speed and power trade-offs in datapath – design time power reduction techniques, run time power reduction, reductions in standby power	Lab 8
9	*11/12 – 11/18*	Memory and Array Structures: SRAM, CAM arrays, Address decoders, sense amplifiers, large/small signal sense amps, timing and control. Memory Reliability and yield, power dissipation in memories, data retention power, minimum operating voltage	Lab 9
10	*11/19 – 11/25*	DNN Domain Specific Architecture components: Matrix Multiplication in TPU, Processing in Memory (PIM)	Lab 10
11	*11/26 – 12/2*		
12	*12/3 – 12/13*	*Review for Final*	**Final Exam, Mon Dec 16th**

Policy on Academic Honesty:

In pursuing these goals, NYU expects and requires its students to adhere to the highest standards of scholarship, research and academic conduct. Essential to the process of teaching and learning is the periodic assessment of students' academic progress through measures such as papers, examinations, presentations, and other projects. Academic dishonesty compromises the validity of these assessments as well as the relationship of trust within the community. Students who engage in such behavior will be subject to review and the possible imposition of penalties in accordance with the standards, practices, and procedures of NYU and its colleges and schools. Violations may result in failure on a particular assignment, failure in a course, suspension or expulsion from the University, or other penalties.

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Moses Center Statement of Disability:

If you are student with a disability who is requesting accommodations, please contact New York University's Moses Center for Students with Disabilities at 212-998-4980 or mosescsd@nyu.edu. You must be registered with CSD to receive accommodations. Information about the Moses Center can be found at www.nyu.edu/csd. The Moses Center is located at 726 Broadway on the 2nd floor.