Gate-first inversion-type InP metal-oxide-semiconductor field-effect transistors with atomic-layer-deposited Al$_2$O$_3$ gate dielectric
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Gate-first inversion-type InP metal-oxide-semiconductor field-effect transistors with atomic-layer-deposited Al2O3 gate dielectric

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We present n-channel enhancement-mode inversion-type indium phosphide (InP) metal-oxide-semiconductor field-effect transistors with atomic-layer-deposited Al2O3 gate dielectric. It has been found that applying sulfur passivation and postdeposition annealing in the process improves the drive current and subthreshold swing. Transistors on semi-insulating InP substrates show much higher drive current than the ones on p-type InP due to the asymmetric distribution of interface state along the bandgap between InP and Al2O3. The effects of transient and slow traps on the transistor performance have also been investigated using constant electrical stress measurements and pulse measurements. © 2008 American Institute of Physics.

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During the past few decades, great efforts have been made to develop III-V based metal-oxide-semiconductor field-effect transistors (MOSFETs) due to the higher electron mobility of III-V materials compared to silicon. The main obstacle to III-V based MOSFET devices is the lack of high quality, thermodynamically stable gate oxides which can passivate the oxide/substrate interface. Recently, various high-k gate dielectrics have been demonstrated on III-V MOS capacitors (MOSCAPs) and MOSFETs, including in situ passivation of GaAs interface with silicon (Si) interface control layer grown by molecular beam epitaxy (MBE), 1 physical vapor deposited Si or germanium (Ge) as interfacial passivation layer between GaAs and the dielectrics, 2,3 in situ MBE deposition of Ga2O3-Gd2O3 mixture or Gd2O3 on III-V substrates, 4 and atomic-layer deposition (ALD) of Al2O3 directly on III-V substrates. 5

Inversion-type MOSFETs prevail over depletion-type MOSFETs because of their superior immunity to drain-induced-barrier-lowering effects, punch-through leakage and breakdown problems. Some progress has been made on inversion-type III-V MOSFETs including GaAs MOSFETs with Si or Ge passivation layer and HfO2 dielectrics, 6,7 or with MBE Ga2O3 (Gd2O3) dielectrics, 8,9 InGaAs MOSFETs with ALD Al2O3 dielectrics, 10–12 or with Si passivation layer and HfO2 dielectrics, 13 or with MBE Ga2O3 (Gd2O3) dielectrics, 14 and InP MOSFETs with ALD Al2O3 dielectrics. 15,16 GaAs inversion-type MOSFETs usually have problems of low drive current [e.g., 162 μA/mm (Ref. 7)], 400 μA/mm (Ref. 8), 500 μA/mm (Ref. 17)]. While InGaAs MOSFETs can provide larger drive current [e.g., 400 μA/mm (Ref. 11) and 1 A/mm (Ref. 12)], they also exhibit relatively high off-current density [e.g., 5×10−4 mA/mm (Ref. 11)], small current on-off ratio [e.g., <104 (Ref. 11) 150 (Ref. 12)] and large subthreshold swing (SS) [e.g., 240 mV/decade (Ref. 11) and 330 mV/decade (Ref. 12)]. On the other hand, InP inversion type MOSFETs with ALD Al2O3 have shown the capability of high drive current density [e.g., 70 mA/mm for 0.75 μm gate length 15], and much smaller off-current density due to larger bandgap (1.34 eV) compared to InGaAs (0.74 eV for In0.53Ga0.47As). In this paper, we have systematically studied the effects of sulfur (S) passivation, postdeposition annealing (PDA), and substrate doping type on device characteristics of inversion-type InP NMOSFETs. The influence of transient and slow charge trapping in the gate stack has also been investigated.

MOSFETs were fabricated on InP (100) substrate with a ring-type structure. 7 The native oxides were removed with a 1% HF solution, then for some samples, S passivation was performed by dipping in a 20% (NH4)2S water solution at room temperature for 10 min. 18 After surface treatment, a 10 nm Al2O3 was deposited by ALD with trimethylaluminum and H2O as precursors at 250 °C. Some samples underwent a PDA at 500 °C in N2 for 5 min. After TaN gate electrode deposition and gate patterning, a Si ion implantation (1×1014/cm2 at 35 keV) was performed for n+ source/drain extension, followed by a high temperature rapid thermal annealing (RTA) at 750 °C for 20 s to activate the implanted dopant in nitrogen ambient. The Ohmic source/drain contacts were made using the evaporation of AuGe/Ni/Au and a conventional lift-off process, followed by RTA at 450 °C for 30 s in nitrogen ambient.

Table I compares the characteristics of MOSFETs on SI-InP substrates with or without S passivation and PDA by listing the threshold voltage (Vth), drive current density (Id), maximum transconductance (gmsmax), and (SS). It has been found that transistors with S passivation show more than two times higher drive current density and much smaller SS. These improvements probably can be attributed to the better thermal stability of the samples with S passivation. 19 PDA at 500 °C for 5 min also improves the transistor characteristics by reducing electron traps in the oxide layer during heat treatment. 19

Besides the fabrication process, substrate doping type is another determining factor for device performance. Figs. 1(a) and 1(b) compare the IdVth curves for MOSFETs on both SI-InP and p-InP substrates. The Vth is around 0.2 V for SI-InP substrates and 1.2 V for p-InP substrates. Ith is of 32
mA/mm for SI-InP and 0.23 mA/mm for p-InP were obtained ($L=4\mu m$, $V_{th}=V_{th}+2\ V$ and $V_d=2\ V$).

To explain the different $I$-$V$ characteristics between SI-InP and p-InP substrates, we plotted the typical C-V characteristics of TaN/Al$_2$O$_3$/InP MOSCAPs at different frequencies from 10 kHz to 1 MHz for both n-InP and p-InP substrates in Fig. 2. One can see that the C-V curve of n-InP substrate shows small frequency dispersion (<5%) at the accumulation region. It has a small bump in the depletion region at 10 KHz, which can be explained by slow interface trap levels. The C-V curve of p-InP MOSCAPs has large stretch out. It has been found that the C-V curve at various frequencies of n-type substrate reflects interface state density above the middle gap while for the p-type substrates, the C-V curve reflects interface state density below the middle gap. Above results suggest that the ALD Al$_2$O$_3$ on InP system has asymmetric distribution of interface state along the bandgap, less interface state density above the midgap than below the midgap. This can be the main reason why SI-InP MOSFETs have much higher drive current and transconductance than p-InP.

The effective mobility has been calculated over entire gate voltage range using split C-V method. 1 MHz C-V curve between gate and channel exhibits an equivalent oxide thickness (EOT) of 4.9 nm and the maximum electron mobility of 410 cm$^2$/V·s (Fig. 3) for SI-InP MOSFETs ($W/L=400/4\ \mu m$).

Figure 4 shows the threshold voltage shift and the normalized drive current drift for 400/4 $\mu m$ ($W/L$) MOSFETs on SI-InP substrate with constant electrical stress fields of $(V_g-V_{th})/EOT=4\ \text{MV/cm}$. The flatband voltage $V_{fb}$ of 0.15 V is extrapolated from the 1 MHz split-CV (inset of Fig. 3). The $V_{th}$ shift of less than 0.1 V after 1000 s stress is obtained. The drive current shows less than 2% deduction after 1000 s stress, indicating much more stable MOSFETs characteristics than earlier results. To suppress the effect of interface states and bulk traps, and reveal more intrinsic device characteristics, the pulsed $I_d/V_g$ under the 50 KHz gate pulse is compared to the dc measurement results for SI-InP MOSFETs ($W/L=400/4\ \mu m$) in Fig. 5. The inset shows the circuit configuration for pulse measurement. The $V_d$ of the MOSFETs for both dc and pulse measurement was normalized to 0.1 V. In dc measurement, the gate stack traps more electrons at the interface or in the gate stack, degrading the electron mobility and drive current. The dc measurement shows peak transcon-

<table>
<thead>
<tr>
<th>Process</th>
<th>MOSFET characteristics</th>
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<tr>
<td>Sulfur passivation</td>
<td>PDA</td>
</tr>
<tr>
<td>A</td>
<td>No</td>
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<td>B</td>
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TABLE I. Effects of sulfur passivation and PDA on MOSFETs characteristics ($W=400\ \mu m$ and $L=8\ \mu m$)

FIG. 1. (Color online) (a) dc $I_d/V_g$ curve at $V_d=0.05\ V$ for MOSFETs on SI-InP and p-InP substrates. (b) dc $I_d/V_g$ characteristics as a function of gate bias MOSFETs on SI-InP and p-InP substrates. The gate bias is varied from $V_{th}$ to $V_{th}+2\ V$ with 0.5 V step.

FIG. 2. (Color online) C-V characteristics of TaN/Al$_2$O$_3$/InP as a function of frequency for both n-InP substrate and p-InP substrate. The thickness of Al$_2$O$_3$ is 10 nm.
ductance of 2.9 mS/mm while pulse $V_g$ provides 11.6 mS/mm.

In conclusion, gate-first $n$-channel enhancement-mode inversion-type MOSFETs have been demonstrated with ALD Al$_2$O$_3$ dielectric on InP substrate. Applying S passivation and PDA can improve the drive current density and SS. The drive current densities of 32 and 0.23 mA/cm electrical stress. Four times higher transconductance is observed with 50 kHz pulse $I_d$-$V_g$ measurement than dc data.

FIG. 3. (Color online) Calculated effective electron mobility as a function of gate voltage for SI-InP MOSFETs. Inset: 1 MHz C-V curve between gate and channel.

FIG. 4. (Color online) Threshold voltage shift and normalized drive current drift under constant voltage stress of ($V_g$-$V_{th}$)/$EOT=4$ MV/cm for SI-InP MOSFETs. Flatband voltage $V_{fb}$ of about 0.15 V was extracted from 1 MHz split C-V in Fig. 3. $V_{th0}$ and $I_{th0}$ are the threshold voltage and the drive current of the fresh devices.

FIG. 5. (Color online) dc and pulse $I_d$-$V_g$ for SI-InP MOSFETs. The frequency of gate pulse is 50 kHz.