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Citation: Applied Physics Letters 97, 213506 (2010); doi: 10.1063/1.3521284
View online: http://dx.doi.org/10.1063/1.3521284
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/97/21?ver=pdfcov
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Hall mobility measurements in enhancement-mode GaAs field-effect transistors with Al2O3 gate dielectric

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(Received 3 October 2010; accepted 5 November 2010; published online 24 November 2010)

We report the direct measurement of the inversion charge density and electron mobility in enhancement-mode n-channel GaAs transistors using gated Hall bars. The Hall data reveal the existence of a reduced mobile charge density in the channel due to significant charge trapping. The peak electron mobility was found to be relatively high (≈2140 cm²/V s), in agreement with inherent high carrier mobility of electrons in III-V materials. © 2010 American Institute of Physics.

[doi:10.1063/1.3521284]

Although fabrication of enhancement-mode (E-mode) III-V metal-oxide-semiconductor field-effect transistors (MOSFETs) has been pursued for several decades,1–3 recently there has been renewed interest in exploring these materials as potential candidates for post-Si complementary metal-oxide-semiconductor applications.4 However, passivation of the interface between gate dielectric and III-V channel materials has long been a key challenge to realize III-V MOSFETs. This, in turn, has driven the research to develop various schemes for interface passivation of III-V materials.5–16 Carrier mobility is a main figure of merit used to benchmark the MOSFET performance, and, therefore, it is important for the carrier mobility to be measured accurately. For example, charge trapping in Si MOSFETs with high-k gate dielectrics can result in the overestimation of inversion charge (Qinv) using conventional split capacitance-voltage (C-V) method17 and charge trapping can influence the calculated effective mobility by distorting the threshold voltages in the measured split C-V and I-V curves.

Despite current progress in passivation of high-k/III-V interface, the reported device characteristics indicate the presence of significant charge traps.5–15 Therefore, to determine the carrier mobility in III-V MOSFETs with high-k gate dielectrics, a direct measurement of Qinv is necessary. Recently, there have been efforts to decouple the contribution of interface traps from the split C-V data for mobility extraction in In0.53Ga0.47As MOSFETs either by conducting the C-V measurements at low temperatures14 or by analyzing the small signal response of the inversion layer using a comprehensive equivalent circuit model.19 In this work, we use gated Hall bars (GHBs) to directly measure Qinv and mobility in E-mode GaAs-channel MOSFETs with Al2O3 gate dielectrics.

Figure 1 shows schematically the GHB structure. The fabrication process for the GHB devices is similar to our previous paper, reporting the fabrication of self-aligned E-mode GaAs n-MOSFETs.10 The GHB transistors were fabricated on (001) undoped semi-insulating GaAs substrates (carbon doped, resistivity ≥1 × 10⁸ Ω cm, bulk mobility ≥4000 cm²/V s). After an ex situ wet clean process using a combination of dilute hydrofluoric acid dip and sulfur passivation in (NH₄)₂S,20 the samples were immediately transferred to an atomic layer deposition (ALD) reactor. Then, an 8.1 nm thick Al₂O₃ layer was grown using trimethylaluminum precursor, which has been shown to effectively reduce the thickness of GaAs native oxides at the high-k/GaAs interface.20–23 Next, TaN metal gate was sputtered and patterned. Active areas were defined prior to Si implantation in order to isolate the source/drain (S/D) regions and sensing voltage areas. The Si implantation was performed at 35 keV with a dose of 1 × 10¹⁴ cm⁻², followed by S/D activation at 800 °C. Finally, AuGe/Ni/Au Ohmic contacts were evaporated and annealed at 450 °C in N₂ ambient.

The Hall resistance was measured using small amplitude (100 nA), low frequency current flown from source to drain. The magnetic field was swept from −0.3 to 0.3 T while the transverse (Vₓy=Vₓ−Vᵧ) and longitudinal (Vₓz=Vₓ−Vᵧ) voltages were measured at different gate voltages using low frequency lock-in techniques.

The typical IₓₓVᵧ characteristics of the GaAs transistors with a gate length of 20 μm are shown in Fig. 2. The inset
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of Fig. 2 shows the split C-V curves and their corresponding $Q_{\text{inv}}$. The strong frequency dispersion of the C-V data indicates the presence of fast traps. The dispersion of the C-V data by itself renders the conventional effective mobility extraction by split C-V method unreliable due to the frequency dependence of the extracted $Q_{\text{inv}}$. The dispersion in split C-V data can be also seen in several other reports for III-V MOSFETs, revealing the importance of a direct $Q_{\text{inv}}$ measurement. The interface state density ($D_{\text{it}}$) of the devices was estimated from the subthreshold slope model (assuming a uniform distribution of $D_{\text{it}}$ in the upper half of the bandgap for n-MOSFETs) to be $\sim 1 \times 10^{12}$ cm$^{-2}$ eV$^{-1}$. In addition to the interface state traps, slow “border traps” further degrade the current, confirmed by pulsed I-V measurements. Figure 3(a) shows the typical pulsed I-V behavior of our devices for two different pulsed widths. The initial fast drop of the current is due to fast traps. As can be also seen, increasing the charging time results in higher degradation of the drain current. The inset shows the schematic illustration of the pulsed I-V setup. Furthermore, the logarithmic time dependence of the $V_{\text{th}}$ shift (and the drain current degradation in the linear transistor operation regime) is a direct indication of charge trapping in the high-k dielectric, shown in Fig. 3(b). As will be discussed, the presence of the slow traps can further complicate the determination of the channel mobility.

To determine the density of mobile electron charges in the channel, Hall measurements were carried out using the GHB structures. The bottom right inset of Fig. 4(a) shows the timing diagram used for the Hall measurements. This is to primarily alleviate the effect of slow traps during the Hall and four-point measurements. The 60 s hold time after applying $V_{\text{gs}}$ and $I_{\text{d}}$, and before sweeping the magnetic field (B), is to fill the majority (more than 95%) of the traps that will otherwise respond during the magnetic field sweep, where the $V_{\text{xy}}$ and $V_{\text{xx}}$ voltages are measured. Figure 4(a) illustrates the Hall resistance ($R_{\text{H}}=V_{\text{xy}}/I$) as a function of magnetic field for a GaAs GHB, measured at two different gate bias voltages. The linearity of the $R_{\text{H}}$-B curves indicates negligible charge trapping after the hold time. We note that the $R_{\text{H}}$-B curve does not pass through the origin due to the mixing between $V_{\text{xx}}$ and $V_{\text{xy}}$, which can result from rotational misalignment between the pads and/or inhomogeneity in the inversion layer. However, this does not influence the extracted $Q_{\text{inv}}$ as the charge density is evaluated from the slope of $R_{\text{H}}$-B curve using $N_{\text{inv}}=(Q_{\text{inv}}/q)=(dR_{\text{H}}/dB)^{-1}/q$, where $q$ is the electronic charge (inset of Fig. 5). The Hall

FIG. 2. (Color online) The typical $I_{\text{d}}$-$V_{\text{g}}$ characteristics of a GaAs MOSFET with a gate length of 20 μm. The inset shows the corresponding split C-V data and the extracted $Q_{\text{inv}}$, manifesting noticeable frequency dispersion.

FIG. 3. (a) The typical pulsed I-V behavior of our GaAs devices for two different pulse widths, confirming the presence of fast and slow traps. The inset shows the schematic illustration of the pulsed I-V setup. (b) The representative logarithmic time dependence of the $V_{\text{th}}$ shift and the drain current degradation for a GaAs device, indicating charge trapping by border traps in the ALD-Al$_2$O$_3$.

FIG. 4. (Color online) The representative $R_{\text{H}}$-B characteristics for two different $V_{\text{g}}$ values. The inset illustrates the Hall measurement scheme as well as the timing diagram for the test based on which the GHB measurements were carried out.
data show a relatively low $N_{\text{inv}}$ by comparison to the expected values from split $C-V$ data, revealing significant charge trapping in our GaAs transistors. Nevertheless, unlike the split $C-V$ data, which are contaminated by the effect of charge traps, the measured $N_{\text{inv}}$ by the Hall measurements is the true mobile charge density in the channel.

Another advantage of the GHB structure is the elimination of the parasitic effect of the source/drain series resistance on the extracted mobility through four-point measurements. As a result, the intrinsic channel resistance $[R_{\text{ch, int}} = V_{\text{xx}}/I_{\text{d}} = (qN_{\text{inv}} \mu_{\text{FE}})^{-1}]$ was directly measured at different gate voltages. The mobility was evaluated using the extracted mobile charge density in the channel at different gate voltages via Hall measurements, in combination with the corresponding intrinsic channel resistance, shown in Fig. 5. The peak Hall channel mobility was measured to be $\sim 2140$ cm$^2$/V s, consistent with the high intrinsic electron mobility of GaAs. The high mobility of electrons stem from the screening of the scattering sites created by the fast interface states during the Hall mobility measurements. The sufficiently long hold time of 60 s allows the majority of traps to be filled by electrons prior to the sweep of the B-field. Therefore, the Hall mobility measured by this technique indicates the intrinsic mobility of electrons in the channel in the absence of interface traps.

It is notable that the field-effect mobility for our devices (extracted from the slope of their corresponding $I_{\text{d}}$-$V_{\text{g}}$ curves assuming ideal MOSFET equations) was found to be much lower ($\mu_{\text{FE}} \sim 100$ cm$^2$/V s). These data indicate that substantial charge trapping can be the major cause for the significant degradation of the dc characteristics of our high-k III-V transistors, as well as in many other reports in the literature. Furthermore, the normalized drain current of our devices with respect to the channel length, oxide capacitance ($C_{\text{ox}}$), and gate overdrive is comparable to the recent reports for GaAs MOSFETs.\textsuperscript{5–13} Therefore, the findings of this study can explain the relatively low drive current of these devices.

In summary, we demonstrated that charge trapping significantly impacts the mobility extraction using the conventional split $C-V$ method. To overcome this issue, we have directly measured the inversion charge density and the corresponding intrinsic channel mobility for self-aligned inversion-type E-mode high-k GaAs transistors using gated Hall bars. The high mobility of mobile charges in the channel measured using this technique suggests that charge trapping significantly degrades the performance of our high-k III-V transistors.

This work was supported in part by DARPA and Micro Foundation.

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