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EDUCATION

- **Ph.D** in Electrical Engineering, The Ohio State University, Columbus, 5/85.
- **M.S.E.E,** National Chiao Tung University, Taiwan, ROC, 5/80.
- **B.S.E.E,** National Chiao Tung University, Taiwan, ROC, 5/77.

PROFESSIONAL EXPERIENCE

- **NYU,** Dept. of Electrical and Computer Engineering, Brooklyn, NY
  Full Professor: 9/97 – present
  Department Head: 7/04 – 6/14
  Associate Professor: 1/92 – 8/97

  Three of my research projects are briefly described below:

  1. Datacenter Cloud Computing: Leading a team to develop various technologies to support large-scale datacenters, including virtualization, security, traffic engineering, resilience, and energy saving. By working with the researchers at ATT, Bell Labs, and IBM, the team has been doing cutting-edge research and produced several inventions to be transferred to industry.
  2. Ultra Low Power Implant Devices: Leading a team to work with doctors at NYU Medical School and Taiwan Chang Gung Memorial Hospital to develop medical implantable devices to monitor and help treat diseases such as epilepsy, Alzheimer's and Parkinson's. The devices include low-power seizure detection and on-power data acquisition circuits.
  3. Network Security: Led a team to implement high-speed network security functions, including intrusion detection/prevention and distributed denial of service (DDoS) defense systems, on FPGA boards with a target rate of 10 Gbps and beyond. The technologies are to be transferred to industry.

  Courses that I have taught at NYU-Poly:

  1. Data Centers and Cloud Computing (EL9333)
  2. High-Performance Switches and Routers (EL7373), used the switches/routers book I co-authored for the textbook
  3. Network Security Systems Design (EL6393)
  4. High-Speed Networks (EL6383), used the QoS Control book I co-authored for the textbook
  5. Integrated Circuit (VLSI) Design (EL5473)
  6. VLSI System and Architecture Designs (EL6443)

- **Coree Networks, Inc., Tinton Falls, New Jersey, CTO and Founder**: 7/00 – 8/01

    - Took one-year leave of absence from NYU-Poly to start up the company with the first round of $30M venture capital fund. The company closed down in a little over a year due to the downturn of telecom market. It had 95 employees when closing down.
    - Oversaw all research and development activities related to Coree's product line and explored new technologies for terabit IP routers and MPLS switches.
    - Led a team to design a fault-tolerant packet switch system with more than 10 terabit/s capacity and five 9 availability, including the design and modeling of 3 ASIC and 8 FPGA chips.
    - Led a team to investigate different layers of protection/restoration and traffic engineering in the IP/MPLS network.

- **Consultant to Telcordia, NEC, and Lucent at various times during 1/92 – 6/00**

- **Telcordia (Bellcore), Red Bank, New Jersey, Member of Technical Staff**, 5/85 - 1/92
  Involved in the following projects:
    1. ATM Congestion Control
       Implemented a VLSI chip (150 thousand CMOS transistors), called a Sequencer, to shape user traffic from thousands of virtual channels in ATM networks. The chip also facilitates a queue manager that handles multiple delay and loss priorities jointly in ATM switch nodes. The chip has been used in the Aurora Gigabit testbed (by Bellcore, IBM, MIT and University of Pennsylvania).
    2. Nectar Gigabit Network Testbed Project
       Played a key role in designing an architecture for interconnecting gigabit hosts/LANs through SONET/ATM networks, converting HIPPI (High Performance Parallel Interface) packets at Gbit/sec to the SONET/ATM transmission format, and vice versa.
    3. A Large-Scale Modular ATM Switch
       The proposed ATM switch uses a regular and recursive structure to accommodate thousands of input ports, resulting in a capacity over 1 Terabit/sec.
    4. A SONET/ATM-based Optical Customer Premises Network
       A new optical customer premises network, called H-Bus, was designed to interface multiple terminal equipment to an ATM network. To resolve the access contention on the bus, a new multiple-priority media access control (MAC) protocol was devised and implemented with a 1.2-μm CMOS VLSI chip, called an ATM-Layer chip.
    5. A Packet Video/Audio Transmission System
       Prototyped a point-to-point packet transmission system, which statistically multiplexes a video signal and two audio channels. A novel digital phase-locked loop circuit was implemented to recover the service clock that is not carried by the packet network.
    6. A 200 Mbit/s Framer Chip for a B-ISDN System
       Implemented a 2-μm CMOS LSI chip, called a Framer, to support a SONET-like time division multiplexer. Several hundreds of the chip were fabricated and used in trial systems by Regional Bell Companies.
    7. A 2-μm CMOS Regenerative Phase Aligner Chip
       Implemented a 120 Mbit/s Regenerative Phase Aligner (REPA) chip to align the phase of a high-speed data stream to a local system clock.

- **Polytechnic University,** Dept. of Electrical Engineering, Brooklyn, NY
  Adjunct Associate Professor, 9/85 - 12/91

  Developed and taught two courses:
  - Integrated Circuit (VLSI) Design (Basic)
  - VLSI System and Architecture Designs (Advanced)

- **Telecommunication Laboratory, Taiwan, Senior Engineer**, 9/77 - 9/81

  Designed a fault-tolerant microcomputer controller of a local digital switching system; involved in designing and implementing a time-space-time digital switching system.

SERVICES IN UNIVERSITY

1. Chair of Undergraduate Computer Engineering Steering Committee (since 1993) with responsibility of Computer Engineering curriculum and coordination between ECE and Computer Science departments.
2. Chair of ECE Dept Tenure and Appointment Committee.
3. Member of University Tenure and Appointment Committee.
4. Member of University Undergraduate Curriculum Standards Committee.
5. Advise MS Computer Engineering students on their curriculum and handling their admission.

PROFESSIONAL ACTIVITIES

1. Have been serving as Panelist for NSF proposals.

2. General Chair of ACM/IEEE ANCS (Symposium on Architectures for Networking and Communications Systems), Oct. 2011, and HPSR (High-Performance Switching and Routing), May 2007.

3. Editor of IEEE/ACM Trans. on Networking from Aug. 1996 to Sep. 2000.

4. Guest editor of IEEE Journal on Selected Areas in Communications with special topic on "High-Speed Network Security – Architectures, Algorithms, and Implementations" for Oct. 2006 issue.

5. Guest editor of IEEE Journal on Selected Areas in Communications with special topic on "High-Performance Optical/Electronic Switches/Routers for High-Speed Internet" for May and September issues of 2003.

6. Guest editor of IEEE Journal on Selected Areas in Communications with special topic on "Next Generation IP Switches and Routers" published in June 1999.

7. Guest editor of IEEE Journal on Selected Areas in Communications with special topic on "Advances in ATM Switching Systems for B-ISDN," published in June 1997.

8. TPC member of a number of conferences, such as HPSR (High-Performance Switching and Routing), ICC, Globecom, and etc.

INVITED SHORT-COURSES

1. Have given a 3 or 4-day short course several times a year to industry worldwide through the arrangement of UC Berkeley and Oxford University Continuing Education Division for more than 10 years until year 2002. The titles of the short courses are "SONET/ATM Networks" and "IP/MPLS Networks."

2. Three-day short course, "VLSI Designs for Broadband ISDN," National Chiao Tung University, Taiwan, July 1988.

HONORS AND AWARDS

1. Elected to be Fellow of National Academy of Inventors (NAI) for "having demonstrated a highly prolific spirit of innovation in creating or facilitating outstanding inventions that have made a tangible impact on quality of life, economic development, and the welfare of society," Dec 2014.

2. Elected to be Speaker of the Year by IEEE New Jersey Coast Section, April 2003.

3. Elected to be Fellow of IEEE for contributions to the architecture and application of VLSI circuits in high-speed packet networks in January 2001.

4. Co-recipient of the journal's best paper award of 2001 IEEE Transactions on Circuits and Systems for Video Technology.

5. Received Bellcore Excellence Award in March 1987 for designing the first SONET-like Frame chip running up to 200 Mbit/s using CMOS 2-μm technology.

BOOKS

1. Broadband Packet Switching Technologies – A Practical Guide to ATM Switches and IP Routers, H. J. Chao, C. Lam, and E. Oki, published by John Wiley & Sons, Inc, in Sep. 2001.

2. Quality of Service Control in High-Speed Networks, H. J. Chao and X. Guo, published by John Wiley & Sons, Inc, in Nov. 2001.

3. High Performance Switches and Routers, H. J. Chao and B. Liu, published by John Wiley & Sons, Inc, in April 2007.

PATENTS

1. M. Beckner, H. J. Chao, and T. Robe, "Framer circuit for use in DTDM (Dynamic Time-Division Multiplexing) network," patent no. 4,819,226, issued in Apr. 1989.
2. H. J. Chao and S. Lee, "Time division multiplexer for DTDM bit streams," patent no. 4,833,673, issued in May 1989.
3. H. J. Chao, "DTDM multiplexer with cross-point switch," patent no. 4,855,999, issued in Aug. 1989.

4. H. J. Chao, S. Lee, and L. Wu, "Method and apparatus for multiplexing circuit and packet traffic," patent no. 4,893,306, issued in Jan. 1990.
5. H. J. Chao and C. Johnston, "Service clock recovery circuit," patent no. 5,007,070, issued in Apr. 1991.
6. H. J. Chao, G. Shtirmer, and L. S. Smoot, "Optical customer premises network," patent no. 5,050,164, issued in Sep. 1991.
7. H. J. Chao, G. Shtirmer, and L. S. Smoot, "Customer premises network node access protocol," patent no. 5,079,763, issued in Jan. 1992.
8. H. J. Chao, "Grouping network based non-buffer statistical multiplexer," patent no. 5,124,978, issued in June 1992.
9. H. J. Chao, "Crosspoint matrix switching element for a packet switch," patent no. 5,179,552, issued in Jan. 1993.
10. H. J. Chao, "Distributed modular packet switch employing recursive partitioning," patent no. 5,197,064, issued in Mar. 1993. This patent has been licensed to AT&T.
11. H. J. Chao and C. Johnston, "Service clock recovery for variable bit rate services," patent no. 5,204,882, issued in Apr. 1993. This patent has been licensed to AT&T.
12. H. J. Chao, "Method and system for managing queued cells," patent no. 5,278,828, issued in Jan. 1994. This patent has been licensed to AT&T.
13. H. J. Chao, "B-ISDN Sequencer chip device," patent no. 5,313,579, issued in May 1994.
14. H. J. Chao, "Method and system for controlling user traffic to a fast packet switching system," patent no. 5,381,407, issued in Jan. 1995.
15. H. J. Chao and B. S. Choe, "Scalable multicast ATM switch," patent no. 5,724,351, issued in March 1998.
16. H. J. Chao and N. Uzun, "ASIC chip for implementing a scalable multicast ATM switch," patent no. 5,790,539, issued in Aug. 1998.
17. H. J. Chao and X. Guo, "Methods and apparatus for handling time stamp aging," patent no. 6,081,507, issued in June 2000.
18. H. J. Chao and Y. R. Jenq, "Methods and apparatus for shaping queued packets using a two-dimensional RAM-based search engine," patent no. 6,370,144, issued on April 9, 2002.
19. H. J. Chao and Y. R. Jenq, "Methods and apparatus for fairly scheduling queued packets using a RAM-based search engine," patent no. 6,389,031, issued on May 14, 2002.
20. H. J. Chao and A. Altinordu, "Methods and apparatus for providing a fast ring reservation arbitration," patent no. 6,449,283, issued on Sep. 10, 2002.
21. H. J. Chao, "Methods and apparatus for fairly arbitrating contention for an output port," patent no. 6, 487, 213, issued on Nov. 26, 2002.
22. H. J. Chao and J. S. Park, "Methods and apparatus for arbitrating output port contention in a switch having virtual output queueing," patent no. 6,667,984, issued on Dec. 23 2003.
23. H. J. Chao, E. Oki, and R. Rojas-Cessa, "Scheduling the dispatch of cells in non-empty virtual output queues of multistage switches using a pipelined arbitration scheme," patent no. 6,940,851, filed on July 23, 2001, issued on Sep. 6, 2005.
24. H. J. Chao, E. Oki, and R. Rojas-Cessa, "Pipelined maximal-sized matching cell dispatch scheduling," patent no. 7,006,514, filed on June 1, 2001, issued on Feb. 28, 2006.
25. H. J. Chao, E. Oki, and R. Rojas-Cessa, "Scheduling the dispatch of cells in non-empty virtual output queues of multistage switches using a pipelined hierarchical arbitration scheme," patent no. 7,046,661, filed on July 23, 2001, issued on May 16, 2006.
26. H. J. Chao and E. Oki, "Scheduling the dispatch of cells in multistage switches using a hierarchical arbitration scheme for matching non-empty virtual output queues of a module with outgoing links of the module," patent no. 7,103,056, filed on June 1, 2001, issued on September 5, 2006.

27. H. J. Chao and E. Oki, "Scheduling the dispatch of cells in multistage switches," patent no. 7,173,931, filed on May 8, 2001, issued on Feb. 6, 2007.
28. H. J. Chao, Y. Li, and S. S. Panwar, "Arbitration using dual round robin with exhaustive service of winning virtual output queue," patent no. 7,203,202, filed on Oct. 31, 2002, issued on April 10, 2007.
29. W. Lau, M. C. Chuah, Y. Kim, and H. J. Chao, "Distributed architecture for statistical overload control against distributed denial of service attacks," U.S. Patent No. 7,526,807, filed on Nov. 26, 2003, issued on Apr. 28, 2009.
30. J. Joung, W. J. Park; Guansong Zhang, H. J. Chao, "Packet classification apparatus and method using field level tries," U.S. patent no. 7,415,020, filed on February 27, 2004, issued on March 2010.
31. H. J. Chao and J. S. Park, "Maintaining packet sequence using cell flow control," patent no. 7,688,816, filed on Dec. 3, 2004, issued on March 2010.
32. H. J. Chao and J. S. Park, "Packet-level multicasting," U.S. patent no. 7,724,738, filed on June 18, 2004, issued on May 25, 2010.
33. H. J. Chao and K. Xi, "Determining rerouting information for double-link failure recovery in an Internet protocol network," U.S. Patent number 7,738,365, filed on Nov. 2, 2007, issued on June 15, 2010.
34. H. J. Chao and K. Xi, "Rerouting for double-link failure recovery in an Internet protocol network," US patent no. 7,801,031, filed on Nov. 2, 2007, issued on 9/2/2010.
35. H. J. Chao and J. S. Park, "Switch module memory structure and per-destination queue flow control for use in a packet switch," U.S. patent no. 7,869,348, filed on Feb. 11, 2004, issued on 9/7/2010.
36. S. Artan and H. J. Chao, "Generating a hierarchical data structure associated with a plurality of known arbitrary-length bit strings used for detecting whether an arbitrary-length bit string input matches one of a plurality of known arbitrary-length bit strings," U.S. patent no. 7,805,460, filed on October 26, 2007, issued on Sept. 28, 2010.
37. H. J. Chao, S. S. Panwar, and Y. Shen, "Low complexity scheduling algorithm for buffered crossbar switch with 100% throughput," U.S. patent no. 7,852,866, filed on Dec. 31, 2007, issued on Dec. 14, 2010.
38. H. J. Chao and J. S. Park, "Packet reassembly and deadlock avoidance for use in a packet switch," U.S. patent no. 7,852,829, filed on June 18, 2004, issued on 12/14/2010.
39. S. Artan and H. J. Chao, "Generating a boundary hash-based hierarchical data structure associated with a plurality of known arbitrary-length bit strings and using the generated hierarchical data structure for detecting whether an arbitrary-length string input matches one of a plurality of known arbitrary-length bit strings," U.S. patent no. 7,868,792, filed on Feb. 5, 2009, issued on Jan. 11, 2011.
40. H. J. Chao and K. Xi, "Determining rerouting information for single-link failure recovery in an Internet protocol network," U.S. patent no. 7,869,348, filed on April 10, 2007, issued on Jan. 11, 2011.
41. H. J. Chao and K. Xi, "Determining rerouting information for single-node failure recovery in an Internet protocol network," US patent mo. 7,876,672, filed on April 10, 2007, issued on Jan. 25, 2011.
42. H. J. Chao and J. S. Park, "Packet sequence maintenance with load balancing, and head-of-line blocking avoidance in a switch," U.S. patent no. 7,869,348, filed on Feb. 11, 2004, issued on 2/22/2011.
43. S. Artan and H. J. Chao, "Detecting whether an arbitrary-length bit string input matches one of a plurality of known arbitrary-length bit strings using a hierarchical data structure," U.S. patent no. 8,191,142, filed on October 26, 2007, issued on May 29, 2012.
44. S. Artan and H. J. Chao, "Generating a Log-Log hash-based hierarchical data structure associated with a plurality of known arbitrary-length bit strings used for detecting

whether an arbitrary-length string input matches one of a plurality of known arbitrary-length bit strings," U.S. patent no. 8,212,695, filed on Feb. 5, 2009, issued on July 3rd, 2012.

45. H. J. Chao and H. Sun, "Providing a high-speed defense against distributed denial of service (DDoS) attacks," U.S. patent no. 8,248,946, filed on June 6, 2006, issued on Aug. 21, 2012.
46. J. Gong, C. Zhan, H. Chen, R. Hu, J. Zhang, H. J. Chao, H. Su, X. Wang, and T. Sun, "Method for selecting hash function, method for storing and searching routing table and devices thereof," U.S. patent no. 8,325,721, filed on July 29, 2009, issued on Dec. 4th, 2012.
47. M. Bando, Artan, S. and H. J. Chao, "Configuring state machines used to order and select matching operations for determining whether an input string matches any of at least one regular expression using lookahead finite automata based regular expression detection," U.S. patent no. 8,554,698 B2, filed on Oct. 18, 2010, issued on Oct. 8, 2013.
48. M. Bando, Artan, S. and H. J. Chao, "Determining whether an input string matches at least one regular expression using lookahead finite automata based regular expression detection," U.S. patent no. 8,566,344, filed on Oct. 18, 2010, issued on Oct. 22, 2013.
49. M. Bando and H. J. Chao, "Hash-based prefix-compressed tries for IP route lookup," U.S. patent no. 8,625,604, filed on Dec. 1, 2010, issued on Jan. 7, 2014.
50. H. Jonathan Chao and Yang Xu, "Updating A Perfect Hash Data Structure, Such As A Multi-Dimensional Perfect Hash Data Structure, Used For High-Speed String Matching," U.S. patent no. 8,775,393 B2, filed on 03/01/2012, issued on July 8, 2014.
51. M. Bando and H. J. Chao, "Updating prefix-compressed tries for IP router lookup," U.S. patent no. 8,780,926 B2, filed on Dec. 1, 2010, issued on July 15, 2014.
52. H. Jonathan Chao and Yang Xu, "Encoding Non-Deterministic Finite Automaton States Efficiently In a manner that permits simple and fast union operations," U.S. Utility Patent Number: 8,862,585B2, Filed on 10/10/2012, issued on Oct. 14, 2014.
53. S. Artan and H. J. Chao, "Detecting whether an arbitrary-length bit string input matches one of a plurality of known arbitrary-length bit strings using a hierarchical data structure," U.S. patent no. 8,866,644, filed on October 26, 2007, issued on Oct. 21, 2014.
54. H. Jonathan Chao and Kang Xi, "Balancing load in a network, such as data center networking, using flow based routing," U.S. patent no. 8,879,397 B2, filed on May 13, 2011, issued on Nov. 4, 2014.
55. Kang Xi and H. Jonathan Chao, "Dynamically provisioning middleboxes", U.S. patent no. 8,923,294 B2, filed on Jun 28, 2011, issued on Dec. 30, 2014.
56. H. Jonathan Chao and Yang Xu, "Regrouping Non-Deterministic Finite Automaton Active States to Minimize Distinct Subsets", U.S. patent no. 8,935,250 B2, Filed on 10/10/2012, issued on Jan. 13, 2015.
57. H. Jonathan Chao and Yang Xu, "Using a tunable finite automaton for regular expression matching," U.S. patent no. 8,938,454 B2, Filed on 10/10/2012, issued on Jan. 20, 2015.
58. H. Jonathan Chao, Rihua Wei, and Yang Xu, "Finding nonequivalent classifiers to reduce ternary content addressable memory (TCAM) usage," U.S. patent no. 9,094,350 B2, Filed on 3/15/2013, issued on July 28, 2015.
59. H. J. Chao and K. Xi, "IP fast reroute for shared risk link group (SRLG) failure recovery," filed in June 2009, Pending.
60. H. Jonathan Chao and Yang Xu, "Generating Progressively A Perfect Hash Data Structure, Such As A Multi-Dimensional Perfect Hash Data Structure, And Using The Generated Data Structure For High-Speed String Matching," U.S. Utility Patent, Application Number: 13409947, filed on 03/01/2012, Pending.

61. H. Jonathan Chao and Yang Xu, "Generating A Tunable Finite Automaton For Regular Expression Matching," U.S. Utility Patent, Application Number: 13648432, Filed on 10/10/2012, Pending.
62. M. Luo, J. Zhang, and K. Xi, H. J. Chao, W. Chou, "Apparatus for hybrid routing in SDN networks to avoid congestion and achieve good load balancing under fluctuating traffic load," filed on 4/24/2014.
63. H. Jonathan Chao and Yang Xu, "Controlling the reactive caching of wildcard rules for packet processing, such as flow processing in software-defined networks," filed in Aug. 2014.
64. M. Luo, C.Y. Chu, K. Xi, H. J. Chao, and W. Chou, "Partial software defined network switch replacement in IP network," filed in Dec. 2014.

JOURNAL PUBLICATIONS and BOOK CHAPTERS

1. R. Wei, Y. Xu, and H. J. Chao, "Finding Nonequivalent Classifiers in Boolean Space to Reduce TCAM Usage," IEEE/ACM Transactions on Networking (TON), *Volume: 24, Issue: 2*, pp. 968-981, Apr. 2016.
2. Y. Xia, M. Hamdi, and H. J. Chao, "A Practical Large-capacity Three-stage Buffered Clos-network Switch Architecture," IEEE Transactions on Parallel and Distributed Systems, *Volume: 27, Issue: 2*, pp. 317-328, Feb. 2016.
3. Junjie Zhang, Kang Xi and H. Jonathan Chao, "Load Balancing using Generalized Destination-based Multipath Routing," IEEE/ACM Transactions on Networking (TON), *Volume: 23, Issue: 6*, pp. 1959-1969, Dec. 2015.
4. Zehua Guo, Yang Xu, Marco Cello, Junjie Zhang, Zicheng Wang, Mingjian Liu, and H. Jonathan Chao, "JumpFlow: Reducing Flow Table Usage in Software-Defined Networks," Elsevier Computer Networks, Vol. 92, Part 2, December 2015, pp. 300–315.
5. Yen-Chia Chu, N. Sertac Artan, Le-Ren Chang-Chien, H. Jonathan Chao, "High-Efficiency High-Current Drive Power Converter IC for Wearable Medical Devices," IEICE Electronics Express, Vo. 12, No. 24, pp. 1-6, Dec. 2015.
6. Z. Guo, Z. Duan, Y. Xu, and H. J. Chao, "JET: Electricity Cost-aware Dynamic Workload Management in Geographically Distributed Datacenters," Elsevier Computer Communications, Special issue on Green Networking, Volume 50, pp. 162 – 174, September 2014.
7. Zehua Guo, Mu Su, Yang Xu, Zhemin Duan, Luo Wang, Shufeng Hui, and H. Jonathan Chao. "Improving the Performance of Load Balancing in Software-Defined Networks through Load Variance based Synchronization," Elsevier Computer Networks, Volume 68, August 2014, pp. 95–109 .
8. I. Widjaja, A. Walid, Y. Luo. Y. Xu, and H. J. Chao, "The Importance of Switch Dimension for Energy-Efficient Datacenter Networks," Elsevier Computer Communications, Special issue on Green Networking, Volume 50, pp. 152-161, September 2014.
9. Y. Xu, Z. Liu, Z. Zhang, H. J. Chao, "High Throughput and Memory Efficient Multi-Match Packet Classification Based on Distributed and Pipelined Hash Tables," IEEE/ACM Transactions on Networking, vol.22, no.3, June 2014.
10. Y. H. Kao and H. J. Chao, "Design of A Bufferless Photonic Clos Network-on-Chip Architecture," IEEE Trans on Computers, vol. 65, no. 3, March 2014.
11. S. Shukla, S. Chan, A. S.-W. Tam, A. Gupta, Y. Xu, H. J. Chao, "TCP PLATO: Packet Labelling to Alleviate Time-Out," IEEE Journal on Selected Areas in Communications, vol.32, no.1, pp.65-76, January 2014.

12. Z. Guo, Z. Duan, Y. Xu, H. J. Chao, "Cutting the Electricity Cost for Distributed Data Centers through Smart Workload Dispatching," IEEE Communications Letters, vol.17, no.12, pp.2384-2387, December 2013.
13. Indra Widjaja, Anwar Walid, Yanbin Luo, Yang Xu, H. Jonathan Chao, "Switch Sizing for Energy-Efficient Datacenter Networks", ACM SIGMETRICS Performance Evaluation Review, Volume 41 Issue 3, December 2013.
14. K. Xi, Y. H. Kao and H. J. Chao, "A Petabit Bufferless Optical Switch for Data Center Networks," book chapter of "Optical Interconnects for Future Data Center Networks", Part 3, Pages 135-154, published by Springer, 2013.
15. M. Bando, Y. L. Lin, and H. J. Chao, "FlashTrie: Beyond 100Gbps IP Route Lookup using Hash-based Prefix-Compressed Trie," IEEE/ACM Transactions on Networking, Vol. 20, No. 4, pp. 1262-1275, August 2012.
16. M. Bando, N. Sertac Artan, and H. J. Chao, "Scalable Lookahead Regular Expression Detection System for Deep Packet Inspection," IEEE/ACM Transactions on Networking, Vol. 20, No. 3, pp. 699-714, June 2012.
17. L. Shi, B. Liu, C. Sun, Z. Yin, L. Bhuyan and H. J. Chao, "Load-Balancing Multipath Switching System with Flow Slice," IEEE Transactions on Computers, Vol. 61, No. 3, pp. 350-365, March 2012.
18. Y.-H. Kao, M. Yang, N. Sertac Artan, and H. J. Chao, "CNOC: High-Radix Clos Network-on-Chip," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 30, No. 12, pp. 1897-1910, Dec. 2011.
19. Y. Shen, S. Panwar, and H. J. Chao, "SQUID: A Practical 100% Throughput Scheduler for Crosspoint Buffered Switches," in IEEE/ACM Transactions on Networking, Vol. 18, No. 4, pp. 1119 – 1131, Aug. 2010.
20. M. Rodelgo-Lacruz, C. López-Bravo, F. J. González-Castaño, H. J. Chao, and F. Gil-Castiñeira, "Distributed Resource Scheduling in Not-Aligned Optical Cell Switching," IEEE Transactions on Communications, Vol. 58, No. 4, Apr. 2010.
21. R. Rojas-Cessa, E. Oki, and H. J. Chao, "Maximum and Maximal Weight Matching Dispatching Schemes for MSM Clos-network Packet Switches," IEICE Trans. Commum. Vol. E93-B, No.2, pp. 297-304, February, 2010.
22. Y. Shen, S. Panwar, and H. J. Chao, "Design and Performance Analysis of A Practical Load-Balanced Switch," IEEE Transactions on Communications, Vol. 57, No. 8, pp. 2420 – 2429, Aug. 2009.
23. M. Rodelgo-Lacruz, C. L´opez-Bravo, F. J. Gonz´alez-Casta˜no, and H. J. Chao, "Not-aligned optical cell switching paradigm," IEEE/OSA Journal of Optical Communications and Networking, vol. 1, no. 3, pp. B70-B80, August 2009.
24. M. Rodelgo-Lacruz, C. L´opez-Bravo, F. J. Gonz´alez-Casta˜no, and H. J. Chao, "Min-Cost Max-Flow Characterization of Shared-FDL Optical Switches," IEEE Communications Letters, vol. 13, no. 7, pp. 540-542, July 2009.
25. S. Artan and H. J. Chao, "Design and analysis of a multipacket signature detection system," Int. J. Security and Networks, Vol. 2, Nos. 1/2, pp. 1212 – 136, 2007.
26. P. Ayres, H. Sun, H. Jonathan Chao, and W. C. Lau, "ALPi: A DDoS Defense System for High-Speed Networks," in IEEE Journal on Selected Areas in Communications (JSAC), Special Issue on High-Speed Network Security, pp. 1864-1875, Oct. 2006.
27. Y. Kim, W. Lau, M. C. Chuah, and H. J. Chao, "PacketScore: A statistical Packet Filtering Scheme against Distributed Denial-of-Service Attacks," in IEEE Transactions on Dependable and Secure Computing, pp. 141-155, April-June, 2006.
28. R. Rojas-Cessa, E. Oki, and H. J. Chao, "On the combined input-crosspoint buffered switch and round-robin arbitration," in IEEE Trans. on Communications, vol. 53, Issue 11, pp. 1945-1951, Nov. 2005.

29. S. Y. Liew, G. Hu, and H. J. Chao, “Scheduling algorithms for shared fiber-delay-line optical packet switches, Part I: The single-stage case,” IEEE Journal of Lightwave Technology, April 2005.
30. S. Jiang, G. Hu, S. Y. Liew, and H. J. Chao, “Scheduling algorithms for shared fiber-delay-line optical packet switches, Part II: The 3-stage Clos-Network case,” IEEE Journal of Lightwave Technology, April 2005.
31. F. S. Choa, X. Yu, L. Lin, X. Zhao, J. P. Zhang, Y. Gu, G. Zhang, L. Li, H. Xiang, H. Hadimioglu, H. J. Chao, “An optical packet switch based on WDM technologies,” IEEE Journal of Lightwave Technology, vol. 23, no. 3, pp. 994 – 1014, March 2005.
32. H. J. Chao, Z. Jing, and S. Y. Liew, "Matching Algorithms for Three-Stage Bufferless Clos-Network Switches," (invited), in IEEE Communication Magazine, pp. 46-53, Oct. 2003.
33. H. J. Chao, Z. Jing, and K. Deng, “PetaStar: A petabit photonic packet switch,” in IEEE Journal on Selected Areas in Communications (JSAC), Special Issue on High-Performance Optical/Electronic Switches/Routers for High-Speed Internet, vol. 21, no. 7, pp. 1096-1112, Sep. 2003.
34. R. Rojas-Cessa, E. Oki, and H. J. Chao, “Concurrent fault detection for a multiple-plane packet switch,” in IEEE/ACM Trans. on Networking, vol. 11, no. 4, pp. 616-627, Aug. 2003.
35. D. Jeong, H. J. Chao, and H. Kim, “Multiple delay bounds control algorithm via class-level service curves,” in IEICE Trans. Commun, vol. E85-B, no. 7, pp. 1302-1311, Dec. 2002.
36. E. Oki, Z. Jing, R. Rojas-Cessa, and H J. Chao, “Concurrent round-robin-based dispatching schemes for Clos-network switches,” in IEEE/ACM Trans. on Networking, vol. 10, no. 6, pp. 830-844, Dec. 2002.
37. H. J. Chao, “Next generation routers,” (invited), IEEE Proceeding, vol. 90, no. 9, pp. 1518-1558, Sep. 2002.
38. E. Oki, R. Rojas-Cessa, and H J. Chao, “A pipeline-based maximal-sized matching scheme for high-speed input-buffered switches,” in IEICE Trans. Commun, vol. E85-B, no. 7, pp. 1302-1311, July 2002.
39. J. S. Park and H. J. Chao, “Design and analysis of enhanced Abacus switch,” Computer Communications, vol. 25, no. 6, pp. 577 – 589, April 2002.
40. E. Oki, R. Rojas-Cessa, and H J. Chao, “A pipeline-based approach for a maximal-sized matching scheduling in input-buffered switches,” IEEE Communication Letters, vol. 5, no. 6, pp. 263-265, June 2001.
41. H. J. Chao, C. H. Lam, and X. Guo, “Fast ping-pong arbitration for input-output queued packet switches,” International Journal of Communication Systems, vol. 14, pp. 663-678, June 2001.
42. D. Wu and H. J. Chao, “Buffer management and scheduling schemes for TCP/IP over ATM-GFR,” International Journal of Communication Systems, vol. 14, no. 4, pp. 345-359, John Wiley, May 2001.
43. D. Wu, T. Hou, B. Li, and H. J. Chao, “A per flow based node architecture for integrated services packet networks,” Telecommunication Systems, vol. 17, issue 1/2, pp. 135-160, Kluwer Academic Publishers, May/June 2001.
44. H. Kim and H. J. Chao, “Design of an ATM switch for handoff-support,” ACM/Baltzer Wireless network Journal (WINET), vol. 6, no. 6, pp. 411-419, Dec. 2000.
45. H. J. Chao and T. S. Wang, “An optical interconnection network for terabit IP routers,” IEEE Journal of Lightwave Technology, vol. 18, no. 12, pp. 2095-2112, Dec. 2000.
46. H. J. Chao, “Saturn: A terabit packet switch using dual round-robin,” IEEE Communications Magazine, vol. 38, no. 12, pp. 78-84, Dec. 2000.

47. X. Guo, T. Lee, and H. J. Chao, “Concept of backlog balancing and its application to flow control and congestion control in high-speed networks,” IEICE Trans. Commun. vol. E83-B, no. 9, pp. 2100-2116, Sep. 2000.
48. D. Wu, T. Hou, W. Zhu, H.-J. Lee, T. Chiang, Y.-Q. Zhang, and H. J. Chao, “On end-to-end architecture for transporting MPEG-4 video over the Internet,” IEEE Trans. on Circuits and Systems for Video Technology, vol. 10, no. 6, pp. 923-941, Sept. 2000.
49. D. Wu, T. Hou, B. Li, W. Zhu, Y.-Q. Zhang, and H. J. Chao, “An end-to-end approach for optimal mode selection in Internet video communication: Theory and Application,” IEEE Journal on Selected Areas in Communications (JSAC), Special Issue on Error-Resilient Image and Video Transmission, vol. 18, no. 6, pp. 977-995, June 2000.
50. D. Wu, T. Hou, Z.-L. Zhang, and H. J. Chao, “A framework of architecture and traffic management algorithms for achieving QoS provisioning in integrated services networks,” International Journal of Parallel and Distributed Systems and Networks, ACTA Press, vol. 3, no. 2, pp. 64-81, May 2000.
51. H. J. Chao, et al., “A photonic front-end processor in a WDM ATM multicast switch,” IEEE Journal of Lightwave Technology, vol. 18, no. 3, pp. 273-285, March 2000.
52. D. Wu and H. J. Chao, “Efficient bandwidth allocation and call admission control for VBR service using UPC parameters,” International Journal of Communication Systems, John Wiley, vol. 13, no. 1, pp. 29-50, Feb. 2000.
53. T. Hou, D. Wu, B. Li, T. Hamada, I. Ahmad, and H. J. Chao, “A differentiated services architecture for multimedia streaming in next generation Internet,” Computer Networks, vol. 32, no. 2, pp. 185-209, Elsevier, Feb. 2000.
54. F. S. Choa and H. J. Chao, “All-optical packet routing - architecture and implementation,” Journal of Photonic Network Communications, vol. 1, no. 4, pp. 303-311, 1999.
55. T. Kijkanjanarat and H. J. Chao, “Fast IP routing lookups for high performance routers,” Computer Communications Journal, Sep. 1999.
56. H. J. Chao, Y. R. Jenq, X. Guo, and C. H. Lam, “Design of packet fair queuing schedulers using a RAM-based searching engine,” in IEEE J. Select. Areas Commun., pp. 1105-1126, June 1999.
57. H. J. Chao, X. Guo, C. H. Lam, and T. S. Wang, “A terabit IP switch router using optoelectronic technology,” (invited), The Journal of High speed Networks, vol. 8, no. 1, April 1999.
58. H. J. Chao, A book chapter on ``ATM switching systems for multimedia service,” published by Artech House, Inc., Aug. 98.
59. H. J. Chao, B. S. Choe, J. S. Park, and N. Uzun, “Design and implementation of Abacus switch: A scalable multicast ATM switch,” IEEE J. Select. Areas Commun., vol. 15, no. 5, pp. 830-843, June 1997.
60. H. J. Chao, H. Cheng, Y. R. Jenq, and D. Jeong, “Design of a generalized priority queue manager for ATM switches,” IEEE J. Select. Areas Commun., vol. 15, no. 5, pp. 867-880, June 1997.
61. H. J. Chao and N. Uzun, “An ATM routing and concentration chip for a scalable multicast ATM switch,” IEEE J. Solid-State Circuits, vol. 32, no. 6, pp. 816-828, June 1997.
62. H. J. Chao and J. S. Hong, “Design of an ATM shaping multiplexer with guaranteed output burstiness,” Intl. Journal of Computer System Science & Engineering, Special issue on ATM Switching, vol. 12, no. 2, pp. 131-141. March 1997.
63. F. S. Choa and H. J. Chao, “On the optically transparent WDM ATM Multicast (3M) switches,” in Fiber and Integrated Optics, vol. 15, pp. 109-123, 1996.

64. Y. T. Hou, L. Tassiulas, and H. J. Chao, “A unified overview of implementing ATM-based enterprise local area network for desktop multimedia computing,” in IEEE Commun. Magazine, vol. 34, no. 4, pp. 70, April 1996.
65. H. J. Chao and N. Uzun, “An ATM queue manager with multiple delay and loss priorities,” in IEEE/ACM Trans. on Networking, vol. 3, no. 6, pp. 652-659, Dec. 1995.
66. D. E. Smith and H. J. Chao, “Sizing a packet reassembly buffer at a host computer in an ATM network,” in IEEE/ACM Trans. On Networking, vol. 3, no. 6, pp. 798-808, Dec. 1995.
67. H. J. Chao and B. S. Choe, “Design and analysis of a large-scale multicast output buffered ATM switch,” IEEE/ACM Trans. On Networking, vol. 3, no. 2, pp. 112-138, Apr. 1995.
68. H. J. Chao, D. Ghosal, D. Saha, and A. K. Tripathi, “IP on ATM local area networks,” IEEE Commun. Magazine, Aug. 1994.
69. H. J. Chao and N. Uzun, “A VLSI Sequencer chip for ATM traffic shaper and queue manager,” IEEE J. Solid-State Circuits, vol. 27, no. 11, pp. 1634-1643, Nov. 1992.
70. H. J. Chao and D. E. Smith, “A shared-memory virtual channel queue for ATM broadband terminal adaptor,” Intl. J. Digital and Analog Communication Systems, vol. 5, no. 1, pp. 29-37, January-March 1992.
71. H. J. Chao, “A recursive modular terabit/sec ATM switch,” IEEE J. Select. Areas Commun., vol. 9, no. 8, pp. 1161-1172, Oct. 1991.
72. H. J. Chao and S. C. Liew, “Architecture design for ATM statistical multiplexers,” Intl. J. Digital and Analog Communication Systems, vol. 4, no. 4, pp. 237-248, Oct. 1991.
73. H. J. Chao, “A novel architecture for queue management in the ATM network,” IEEE J. Select. Areas Commun., vol. 9, no. 7, pp. 1110-1118, Sep. 1991.
74. C. A. Johnston and H. J. Chao, “The ATM layer chip: an ASIC for B-ISDN applications,” IEEE J. Select. Areas Commun., vol. 9, no. 5, pp. 741-750, June 1991.
75. H. J. Chao, G. Shtirmer, and L. S. Smoot, “H-Bus: An ATM-based optical customer premises network,” IEEE J. Lightwave Technology, vol. 7, no. 11, pp. 1859-1867, Nov. 1989.
76. H. J. Chao and C. A. Johnston, “Behavior analysis of CMOS D flip-flops,” IEEE J. Solid-State Circuits, vol. 24, no. 5, pp. 1454-1458, Oct. 1989.
77. H. J. Chao and C. A. Johnston, “An ATM packet video transmission system,” SPIE Optical Engineering Journal, vol. 28, no. 7, pp. 781-788, July 1989.
78. H. J. Chao and L. S. Smoot, “Architecture design of an optical customer premises network,” IEE Electronics Letters, vol. 25, no. 13, June 1989.
79. H. J. Chao, C. A. Johnston, and L. S. Smoot, “A packet video/audio system using the asynchronous transfer mode technique,” IEEE Trans. on Consumer Electronics, vol. 35, no. 2, pp. 97-105, May 1989.
80. H. J. Chao, “Design of transmission and multiplexing systems for broadband packet networks,” IEEE J. Select. Areas Commun., vol. 6, no. 9, pp. 1511-1520, Dec. 1988.
81. H. J. Chao, T. J. Robe, and L. S. Smoot, “A 140 Mbit/s CMOS LSI framer chip for a broadband ISDN local access system,” IEEE J. Solid-State Circuits, vol. 23, no. 1, pp. 133-141, Feb. 1988.
82. D. E. Orin, K. W. Olson, and H. J. Chao, “Systolic architecture for computation of the Jacobian for robot manipulators,” a book chapter in Computer Architectures for Robotics and Automation, pp. 39-67, edited by James H. Graham, Gordon and Breach Science Publisher, New York, 1987.
83. H. J. Chao, “The design of control system in time division digital switching system-II,” J. Taiwan Telecommunication Laboratories, vol. 11, no. 1, Apr. 1981.
84. H. J. Chao, “Common channel signaling system in time division digital switching system-II,” J. Taiwan Telecommunication Laboratories, vol. 10, no. 3, November 1980.

CONFERENCE PUBLICATIONS

1. K.Y. Chen, A. Junuthula, I. Siddhrau, Y. Xu, H. J. Chao, "SDNShield: NFV-based Defense Framework against DDoS Attacks on SDN Infrastructure," IEEE IEEE Conference on Communications and Network Security, Oct 2016, Philadelphia, PA.
2. Z. Guo, S. Hui, Y. Xu, H. J. Chao, "Dynamic Flow Scheduling for Power-efficient Data Center Networks," IEEE/ACM, IWQoS, Beijing, China June 2016.
3. C-Y Chu, K. Xi, M. Luo, H. J. Chao, "Congestion-Aware Single Link Failure Recovery in Hybrid SDN Networks," Infocom 2015, Hong Kong, April 2015.
4. J. Zhang, K. Xi, M. Luo, H. J. Chao, "Load Balancing for Multiple Traffic Matrices Using SDN Hybrid Routing," IEEE Conference on High Performance Switching and Routing (HPSR), Vancouver, July 2014.
5. B. Yan, Y. Xu, H. Xing, K. Xi, and H. J. Chao, "CAB: a reactive wildcard rule caching system for software-defined networks," In Proceedings of the third workshop on Hot topics in software defined networking, Chicago, Aug. 2014.
6. J. Zhang, K. Xi, M. Luo, H. J. Chao, "Dynamic Hybrid Routing: Achieve Load Balancing for Changing Traffic Demands", IEEE IWQoS 2014, June 2014.
7. Ken Chia-Han Chiang, N. Sertac Artan, and H. Jonathan Chao, "A Signal-Specific Approach for Reducing SAR-ADC Power Consumption," in IEEE Biomedical Circuits and Systems Conference, (BioCAS 2013),Rotherdam, Netherlands, Oct-Nov, 2013,
8. Y. Xia and H. J. Chao, "On Practical Stable Packet Scheduling for Bufferless Three-Stage Clos-Network Switches, " IEEE Conference on High Performance Switching and Routing (HPSR), Taipei, Taiwan, July 2013.
9. A. Aghdai, F. Zhang, N. Dasanayake, K. Xi, and H. J. Chao, "Traffic Measurement and Analysis in an Organic Enterprise Data Center," IEEE Conference on High Performance Switching and Routing (HPSR), Taipei, Taiwan, July 2013.
10. C-L. Sha, T. Kim, N. S. Artan, and H. J. Chao, "Compression-Ratio-Based Seizure Detection," International Conference of the IEEE Engineering in Medicine and Biology Society, (EMBC 2013), Tokyo, July 2013.
11. T. Kim, N. S. Artan, I. W. Selesnick, and H. J. Chao, "Seizure Detection Methods Using A Cascade Architecture For Real-Time Implantable Devices," International Conference of the IEEE Engineering in Medicine and Biology Society, (EMBC 2013), Tokyo, July 2013.
12. K.Y. Chen, Y. Xu, K. Xi, and H. J. Chao, "Intelligent Virtual Machine Placement for Cost Efficiency in Geo-Distributed Cloud Systems", IEEE International Conference on Communications (ICC), June 2013.
13. I. Widjaja, A. Walid, Y. Luo, Y. Xu, and H. J. Chao, "Small versus Large: Switch Sizing in Topology Design of Energy-Efficient Data Centers", 2013 IEEE 21st International Workshop on Quality of Service (IWQoS '13), Montreal, June 2013.
14. Y-C. Chu, N. S. Artan, D. Czarkowski, and H. J. Chao, "A New Single-Stage AC-DC Converter for Medical Implant Devices," IEEE International Symposium on Circuits and Systems (ISCAS), Beijing, May 2013.
15. N. S. Artan, X. Xu, W. Shi, and H. J. Chao, "Optimizing Analog-To-Digital Converters for Sampling Extracellular Potentials," 34th Annual International Conference of the IEEE Engineering in Medicine and Biology Society, (EMBC 2012), San Diego, CA, Aug-Sep 2012.
16. N. S. Artan, R. C. Patel, C. Ning, and H. J. Chao, "High-Efficiency Wireless Power Delivery for Medical Implants Using Hybrid Coils," 34th Annual International Conference of the IEEE Engineering in Medicine and Biology Society, (EMBC 2012), San Diego, CA, Aug-Sep 2012.

17. T. Kim, N. S. Artan, J. Viventi, and H. J. Chao, “Spatiotemporal Compression for Efficient Storage and Transmission of High-Resolution Electrocorticography Data,” 34th Annual International Conference of the IEEE Engineering in Medicine and Biology Society, (EMBC 2012), San Diego, CA, Aug-Sep 2012.
18. J. Zhang, K. Xi, L. Zhang, H. J. Chao, “Optimizing Network Performance using Weighted Multipath Routing”, ICCCN, July 2012.
19. S.W. Tam, K. Xi, Y. Xu, H. J. Chao, “Preventing TCP Incast Throughput Collapse at the Initiation, Continuation, and Termination”, IEEE IWQoS, June 2012.
20. Y. Xia and H. J. Chao, “Module-Level Matching Algorithms for MSM Clos-Network Switches,” IEEE Conference on High Performance Switching and Routing (HPSR), June 2012.
21. N. Alfaraj, Y. Xu, H. J. Chao, "A Practical and Scalable Congestion Control Scheme for High-Performance Multi-Stage Buffered Switches", IEEE Conference on High Performance Switching and Routing (HPSR), June 2012.
22. Y. H. Lam, S. Zhao, K. Xi, H. J. Chao, “Hybrid Security Architecture for Data Center Networks”, IEEE ICC, June 2012.
23. R. Wei, Y. Xu, H. J. Chao, "Block Permutations in Boolean Space to Minimize TCAM for Packet Classification", in the Proceedings of the 31st Annual IEEE International Conference on Computer Communications (IEEE INFOCOM 2012), mini conference, Orlando, Florida, March 2012.
24. A. S. Tam, K. Xi, and H. J. Chao, “Scalability and Resilience in Data Center Networks: Dynamic Flow Reroute as an Example,” Globecom, Houston, TX, Dec. 2011.
25. Y. Xu, L. Ma, Z. Liu, and H. J. Chao, “A Multi-Dimensional Progressive Perfect Hashing for High-Speed String Matching,” ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS), Brooklyn, Oct. 2011.
26. N. S. Artan, X. Li, R. C. Patel, C. Ning, N. Ludvig, and H. J. Chao, “Multi-Layer Coils for Efficient Transcutaneous Power Transfer,” in *33rd Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC 2011)*, Boston, MA, Aug-Sep 2011.
27. Y. Xia and H. J. Chao, “Distributed 100% Throughput Algorithm for Input-Queued Switches,” 2011 IEEE Workshop on High Performance Switching and Routing, July 2011, Cartagena, Spain.
28. Y. H. Kao and H. J. Chao, “BLOCON: A Bufferless Photonic Clos Network-on-Chip Architecture,” ACM/IEEE International Symposium on Networks-on-Chip, Pittsburg, May 2011.
29. N. Alfaraj, J. Zhang, Y. Xu, and H. J. Chao, “HOPE: Hotspot Congestion Control for Clos Network On Chip,” ACM/IEEE International Symposium on Networks-on-Chip, Pittsburg, May 2011.
30. K. Xi and H. J. Chao, “Enabling Flow-based Routing Control in Data Center Networks using Probe and ECMP,” IEEE International Workshop on Cloud Computing, Shanghai, April, 2011.
31. A. S. Tam, K. Xi, and H. J. Chao, “Use of Devolved Controllers in Data Center Networks,” IEEE Infocom Workshop on Cloud Computing, Shanghai, April, 2011.
32. H. Y. Lam, D. Wang, and H. J. Chao, “A Traffic-aware Top-N Firewall Approximation Algorithm,” IEEE Infocom Workshop on Security in Computers, Networking and Communications, Shanghai, April, 2011.
33. H. J. Chao and K. Xi, “Bufferless Optical Clos Switches for Data Centers”, Optical Fiber Communications (OFC), March 2011.

34. M. Bando, N.S. Artan, R. Wei, X. Guo, H. J. Chao, "Range Hash for Regular Expression Pre-Filtering," ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS), San Diego, Oct. 2010.
35. N. S. Artan, H. Vanjani, G. Vashist, Z. Fu, S. Bhakthavatsala, N. Ludvig, G. Medveczky, and H. J. Chao, "A High-Performance Transcutaneous Battery Charger for Medical Implants," in 32nd Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC 2010), Buenos Aires, Argentina, Aug-Sep 2010.
36. A. Tam, K. Xi, and H. J. Chao, "Leveraging Performance of Data Center Networks by Reactive Reroute," IEEE Hot Interconnects, Google campus, Mountain View, CA, Aug. 2010.
37. K. Xi, H. J. Chao, and C. Guo, "'Recovery from Shared Risk Link Group Failures using IP Fast Reroute," International Conference on Computer Communication Networks, Zurich, Switzerland, Aug. 2010, received the best paper award.
38. A. Zia, S. Kannan, G. Rose and H. J. Chao, "Highly-Scalable 3D CLOS NOC for Many-Core CMPs," International CEWCAS, Montreal, Canada, June 2010.
39. Y.H. Kao, N. Alfaraj, M. Yang, and H. J. Chao, "Design of High-Radix Clos Network on Chip," ACM/IEEE International Symposium on Networks-on-Chip, Grenoble, France, May 2010.
40. M. Bando, N. S. Artan, N. Mehta, Y. Guan and H. J. Chao, "Hardware Implementation for Scalable Lookahead Regular Expression Detection," *Reconfigurable Architectures Workshop (RAW)*, Atlanta, GA, Mar. 2010.
41. M. Bando and H. J. Chao, "FlashTrie: Hash-based Prefix-Compressed Trie for IP Route Lookup Beyond 100Gbps" IEEE Infocom, San Diego, March 2010.
42. H. Sun and H. J. Chao, "RateGuard: A Robust Distributed Denial of Service (DDoS) Defense System," IEEE Globecome, Hawaii, Nov. 2009.
43. A. Tam, K. Xi, and H. J. Chao, "A Fast Reroute Scheme for IP Multicast," IEEE Globecome, Hawaii, Nov. 2009.
44. K. Xi and H. J. Chao, "IP Fast Reroute for Double-Link Failure Recovery," IEEE Globecome, Hawaii, Nov. 2009.
45. M. Bando, S. Artan, and H. J. Chao, "'LaFA: Lookahead Finite Automata for Scalable Regular Expression Detection," Symposium on Architectures for Networking and Communications Systems (ANCS), Princeton, NJ, Oct. 2009.
46. Y. Xu, Z, Liu, Z. Zhang, and H. J. Chao, "An Ultra High Throughput and Memory Efficient Pipeline Architecture for Multi-Match Packet Classification without TCAMs," Symposium on Architectures for Networking and Communications Systems (ANCS), Princeton, NJ, Oct. 2009.
47. M. Bando, S. Artan, and H. J. Chao, "FlashLook: 100-Gbps Hash-Tuned Route Lookup Architecture," IEEE Workshop on High Performance Switching and Routing, Paris, June 2009.
48. M. Rodelgo-Lacruz, C. López-Bravo, F. J. González-Castaño, and H. J. Chao, "Practical Scalability of Wavelength Routing Switches" in IEEE ICC, Germany, June 2009.
49. S. Artan, H. Yuan, and H. J. Chao, "A Dynamic Load-Balanced Hashing Scheme for Networking Applications," IEEE Globecome, New Orleans, LA, Nov. 2008.
50. M. Bando, S. Artan, and H. J. Chao, "Highly Memory-Efficient LogLog Hash for Deep Packet Inspection," IEEE Globecome, New Orleans, LA, Nov. 2008.
51. H. Sun, Y, Zhuang, and H. J. Chao, "A Principal Components Analysis-based Robust DDoS Defense System," IEEE ICC, Beijing, May 2008.
52. S. Artan, M. Bando, and H. J. Chao, "Boundary Hash for Memory-Efficient Deep Packet Inspection," IEEE ICC, Beijing, May 2008.

53. Y. Shen, S. Panwar, and H. J. Chao, “A Low Complexity Scheduling Algorithm for a Crosspoint Buffered Switch with 100% Throughput,” IEEE Workshop on High Performance Switching and Routing, Shanghai, China, May 2008.
54. Y. Huang, H. Sun, H. J. Chao, and X. Chao, “Non-negative Increment Feature Detection of the Traffic Throughput for Early DDoS Attack, “IEEE International Conference on Signal Image Technology and Internet Based Systems, DEC 16-19, 2007.
55. K. Xi and H. J. Chao, “"ESCAP: Efficient SCan for Alternate Paths to Achieve IP Fast Rerouting,” IEEE Globecome, Washington DC, Nov. 2007.
56. S. Artan and H. J. Chao, “A 10-Gbps High-Speed Single-Chip Network Intrusion Detection System,” IEEE Globecome, Washington DC, Nov. 2007.
57. S. Artan, K. Sinkar, J. Pa, and H. J. Chao, “Aggregated Bloom Filters for Intrusion Detection And Prevention Hardware,” IEEE Globecome, Washington DC, Nov. 2007.
58. K. Xi and H. J. Chao, “IP Fast Rerouting for Single-Link/Node Failure Recovery,” IEEE BroadNets, Raleigh, NC, Sept. 2007.
59. W. C. Lau, M. Kodialam, T.V. Lakshman, and H.J. Chao, “DATALITE: a Distributed Architecture for Traffic Analysis via LIght-weight Traffic digEst,” IEEE BroadNets, Raleigh, NC, Sept. 2007.
60. H. J. Chao and J. Park, “Flow control in a multi-plane multi-stage buffered packet switch,” 2007 IEEE Workshop on High Performance Switching and Routing, May 2007, Brooklyn, NY.
61. Y. Shen, S. Panwar, and H. J. Chao, “Performance Analysis of a Practical Load-balanced Switch,” 2007 IEEE Workshop on High Performance Switching and Routing, May 2007, Brooklyn, NY.
62. S. Artan and H. J. Chao, “TriBiCa: Trie Bitmap Content Analyzer for High-Speed Network Intrusion Detection,” IEEE Proc. INFOCOM, Anchorage, Alaska, May 2007.
63. Y. Li, S. Panwar, H. J. Chao, and J. Lee, “Packet Delay-Aware Scheduling in Input Queued Switches,” IEEE GLOBECOM 2006, St. Francisco, CA, Nov. 27-30, 2006.
64. Y. Shen, S. Panwar, and H. J. Chao, “Performance Analysis of a Practical Load Balanced Switch,” IEEE Workshop on High Performance Switching and Routing, Poznan, Poland, June 7-9, 2006.
65. S. Artan and H. J. Chao, “Multi-packet Signature Detection using Prefix Bloom Filters,” in IEEE GLOBECOM, St Louis, MO, Nov. 28-Dec 2, 2005.
66. S. Jiang and H. J. Chao, “Design of Cell Edge Routers in the Optical Cell Switch (OCS) Network,” in IEEE GLOBECOM 2005, St Louis, MO, Nov. 28-Dec 2, 2005.
67. P. Ayres, H. Sun, H. J. Chao, and W. C. Lau, “A Distributed Denial-of-Service Defense System Using Leaky-Bucket-Based PacketScore,” Applied Cryptography and Network Security, ACNS 2005, New York, June 2005.
68. H. J. Chao, J. S. Park, S. Artan, S. Jiang, and G. Zhang, “TrueWay: A highly scalable multi-plane multi-stage buffered switch,” IEEE Workshop on High Performance Switching and Routing, Hong Kong, May 2005.
69. Y. Shen, S. Jiang, S. S. Panwar, and H. J. Chao, “Byte-Focal: a practical load-balanced switch,” IEEE Workshop on High Performance Switching and Routing, Hong Kong, May 2005.
70. S. Y. Liew, G. Hu, H. J. Chao, “Scheduling Algorithms for Shared Fiber-Delay-Line Optical Packet Switches, Part I: The Single-Stage Case,” IEEE GLOBECOM 2004, Dallas, Nov. 2004.
71. T. Ji, H. J. Chao, and N. Feng, “Wireless Coexistence: Pareto Optimality,” IEEE GLOBECOM 2004, Dallas, Nov. 2004.
72. H. J. Chao, R. Karri and W. L. Lau, "CYSEP -- a Cyber-Security Processor for 10Gbps+ Networks," MILCOM, Monterey, CA, Oct. 2004.

73. M. C. Chuah, W. Lau, Y. Kim, and H. J. Chao, "Transient Performance of PacketScore for blocking DDoS attack," *IEEE ICC 2004,* Paris, June 2004.
74. R. Rojas-Cessa, E. Oki, and H. J. Chao, "Maximum Weight Matching Dispatching Scheme in Buffered Clos-network Packet Switches," IEEE ICC 2004, Paris, June 2004.
75. Y. Li, S. Panwar, H. J. Chao, "Exhaustive Service Matching Algorithms for Input Queued Switches," IEEE Workshop on High Performance Switching and Routing, Phoenix, April 2004.
76. Y. Kim, W. Lau, M. C. Chuah, and H. J. Chao, "PacketScore: statistical-based overload control against distributed denial-of-service," IEEE Proc. INFOCOM, Hong Kong, March 2004.
77. S. Y. Liew and H. J. Chao, "Scheduling Algorithms for Shared-Fiber-Delay-Line Optical Cell Switches," Optical Fiber Communications (OFC), Los Angles, Feb. 2004.
78. G. Zhang and H. J. Chao, "Fast Packet Classification Using Field-Level Trie," IEEE Globecom, San Francisco, CA, Dec. 2003.
79. H. J. Chao and S. Y. Liew, "A New Optical Cell Switching Paradigm", International Workshop on Optical Burst Switching, Dallas, TX, Oct. 2003.
80. H. J. Chao, S. Y. Liew, and Z. Jing, "A Dual-Level Matching Algorithm for 3-Stage Clos-Network Packet Switches," HOT Interconnects, Stanford Univ, CA, Aug. 2003.
81. S. Y. Liew and H. J. Chao, "On Slotted WDM Switching in Bufferless All-Optical Networks," HOT Interconnects, Stanford Univ, CA, Aug. 2003.
82. Y. Li, S. Panwar, H. J. Chao, "Frame-based Matching Algorithms for Optical Switches," IEEE Workshop on High Performance Switching and Routing, Torino, Italy, June 2003.
83. H. J. Chao, K. L. Deng, and Z. Jing, "Packet scheduling scheme for a 3-stage Clos-network photonic switch," IEEE ICC 2003, Anchorage, Alaska, May 2003.
84. Y. Kim and H. J. Chao, "Performance of exhaustive matching algorithms for input-queued switches," IEEE ICC 2003, Anchorage, Alaska, May 2003.
85. Y. Kim, J.-Y. Jo, H. J. Chao, and F. L. Merat, "High-speed router filter for blocking TCP flooding under distributed denial of service attack," International Performance, Computing and Communications Conference, Phoenix, Arizona, April 2003.
86. H. J. Chao, K-L. Deng, and Z. Jing, "A Petabit Photonic Packet Switch (P3S)," IEEE INFOCOM, San Francisco, April 1-3, 2003.
87. Y. Li, S. Panwar, and H. J. Chao, "Performance analysis of a dual round robin matching switch with exhaustive service," IEEE Globecom, Taiwan, Nov. 2002.
88. J.-Y. Jo, Y. Kim, and H. J. Chao, "TCP performance comparison under various load balancing methods using OPNET," OPNETWORK, Washington, DC, Aug. 2002.
89. J.-Y. Jo, Y. Kim, H. J. Chao, and F. L. Merat, "Internet traffic load balancing using dynamic hashing with flow volume," SPIE ITCom 2002, Boston, MA, July 2002.
90. Y. Li, S. Panwar, and H. J. Chao, "The dual round robin matching switch with exhaustive service," IEEE Workshop on High Performance Switching and Routing, Kobe, May 2002.
91. E. Oki, R. Rojas-Cessa, and H. J. Chao, "PCRRD: A pipeline-based concurrent round-robin dispatching scheme for Clos-network switches," in IEEE ICC 2002, New York, April 2002.
92. E. Oki, R. Rojas-Cessa, and H. J. Chao, "PMM: A pipelined maximal-sized matching scheduling approach for input-buffered switches," in IEEE Globecom Conference, San Antonio, Texas, Nov. 2001.
93. R. Rojas-Cessa, E. Oki, and H. J. Chao, "CIXOB-k: combined input-crosspoint-output buffered packet switch," in IEEE Globecom Conference, San Antonio, Texas, Nov. 2001.

94. R. Rojas-Cessa, E. Oki, and H. J. Chao, “Fast fault detection for a multiple-plane packet switch,” in IEEE Globecom Conference, San Antonio, Texas, Nov. 2001.
95. R. Rojas-Cessa, E. Oki, Z. Jing, and H. J. Chao, “CIXB-1: combined input-once-cell-crosspoint buffered switch,” IEEE Workshop on High Performance Switching and Routing, Dallas, TX, July 2001.
96. E. Oki, R. Rojas-Cessa, Z. Jing and H. J. Chao, “Concurrent round-robin dispatching scheme in a Clos-network switch,” in IEEE ICC, Helsinki, June 2001.
97. Y. Li, S. Panwar, and H. J. Chao, “On the performance of a dual round-robin switch,” IEEE INFOCOM, vol. 3, pp. 1688-1697, Anchorage, Alaska, April 2001.
98. L. S. Chen and H. J. Chao, “Delay-bound guarantee in combined input-output buffered switches,” IEEE Globecom, San Francisco, Dec. 2000.
99. S. Chang, H. J. Chao, and X. Guo, “TCP-friendly widow congestion control with dynamic grouping for reliable multicast,” in IEEE Globecom, San Francisco, Dec. 2000.
100. D. Wu, Y. T. Hou, Z. L. Zhang, H. J. Chao, and T. Hamada, “A per-flow based node architecture for integrated services packet networks,” in IEEE ICC, New Orleans, Louisiana, June 2000.
101. D. Wu, Y. T. Hou, Y. Q. Zhang, and H. J. Chao, “Optimal mode selection in Internet Video Communication: An end-to-end approach,” in IEEE ICC, New Orleans, Louisiana, June 2000.
102. L. Wu, H. J. Chao, et al., “An FPGA controlled WDM buffer memory,” in CLEO/QELS Conference, San Francisco, May 2000.
103. D. Wu, Y. T. Hou, Y. Q. Zhang, W. Zhu, and H. J. Chao, “Adaptive QoS control for MPEG-4 video communication over wireless channels,” in IEEE Workshop & Exhibition on MPEG-4 (ISCAS'2000), Geneva Switzerland, May 2000.
104. D. Wu, Y. T. Hou, Y. Q. Zhang, and H. J. Chao, “Real-time video streaming over the Internet: A big picture,” in Networld+Interop Engineers Conference, Las Vegas, May 2000.
105. H. J. Chao, X. Guo, and C. H. Lam, “A fast arbitration scheme for terabit packet switches,” in IEEE Globecom, Brazil, Dec.1999.
106. T. Kijkanjanarat and H. J. Chao, “Fast IP lookups using a two-trie data structure,” in IEEE Globecom, Brazil, Dec. 1999.
107. F. S. Choa and H. J. Chao, “Transparent all-optical packet routing - one network for all traffic,” in European Conference on Networks and Optical Communications, Delft, Netherlands, June 22-24, 1999.
108. D. Wu, T. Hou, Z.-L. Zhang, H. J. Chao, T. Hamada, T. Taniguchi, “On implementation architecture for achieving QoS provisioning in integrated services networks,” in IEEE ICC, Vancouver, Canada, June 1999.
109. D. Wu, T. Hou, W. Zhu, Y.-Q. Zhang, H. J. Chao, “MPEG-4 compressed video over the Internet,” in Proc. IEEE International Symposium on Circuits and Systems ISCAS'99), Orlando, FL, May 30 - June 2, 1999.
110. D. Wu and H. J. Chao, “Efficient bandwidth allocation and call admission control for VBR service using UPC parameters,” in IEEE Proc INFOCOM, New York, March, 1999.
111. H. J. Chao and T. S. Wang, “Design of an optical interconnection network for terabit IP router,” in IEEE LEOS, Orlando, Dec.1998.
112. H. J. Chao, et al., “A photonic ATM front-end processor,” in IEEE LEOS, Orlando, Dec. 1998.
113. H. J. Chao and J. S. Park, “Architecture designs of a large-capacity Abacus ATM switch,” in IEEE Globecom, Sydney, Australia, Nov. 1998.
114. D. Wu and H. J. Chao, “Buffer management and scheduling for TCP/IP over ATM-GFR,” in IEEE Globecom, Sydney, Australia, Nov. 1998.

115. H. Kim and H. J. Chao, “Design of a mobility-support ATM switch,” in IEEE Globecom, Sydney, Australia, Nov. 1998.
116. J. Y. Fan, L. M. Wang, Y. Chai, F. S. Choa, H. J. Chao, Z. Zhang, L. Wu, and S. Yang, “A photonic ATM front-end processor,” in ECOC, Sep. 1998.
117. H. J. Chao and J. S. Park, “Centralized contention resolution schemes for a large-capacity optical ATM switch,” in IEEE ATM Workshop Proceeding, Fairfax, VA, May 1998.
118. D. Wu and H. J. Chao, “TCP/IP over ATM-GFR,” in IEEE ATM Workshop Proceeding, Fairfax, VA, May 1998.
119. H. J. Chao and J. S. Park, and T. S. Wang, “Terabit/s ATM switch with optical interconnection network,” in IEEE LEOS, San Francisco, Nov. 1997.
120. H. J. Chao, F. S. Choa, M. H Shih, and T. S. Wang, “A dynamic dense WDM network,” Summer Topical Meeting in Technology for a Global Information Infrastructure, Montreal, Canada, Aug. 1997.
121. H. J. Chao, B.-S. Choe, J.-S. Park and N. Uzun, “Design and implementation of Abacus switch: A scalable multicast ATM switch,” in IEEE Globecom, London, Nov. 1996.
122. H. J. Chao and Y. R. Jenq, “A priority CAM chip for a generic ATM scheduler,” in IEEE ATM Workshop Proceeding, San Francisco, CA, Aug. 1996.
123. H. J. Chao and D. Jeong, “Generalized priority queue manager design for ATM switches,” in IEEE ICC, Dallas, TX, June 1996.
124. H. J. Chao and N. Uzun, “An ATM routing and concentration chip for a scalable multicast ATM switch,” invited to Workshop on Academic Electronics in New York State, Syracuse, New York, June, 1996.
125. H. J. Chao and N. Uzun, “An ATM routing and concentration chip for a scalable multicast ATM switch,” invited to Design SuperCon, Santa Clara, CA, Jan. 1996.
126. H. J. Chao, “Transport technology for interactive TV,” invited talk at Multimedia Symposium, Newark, NJ, Nov. 1995.
127. H. J. Chao, B. S. Choe, and J. S. Park, “Abacus switch: a new scalable multicast ATM switch,” in SPIE Conference on Voice, Video and Data Communications, Philadelphia, PA, Oct. 1995.
128. H. J. Chao, “Advances in ATM switching systems for B-ISDN,” invited talk at Chinese Institute of Engineers (CIE)-USA Annual Convention, Newark, NJ, Sep. 1995.
129. F. S. Choa and H. J. Chao, “Photonics devices and integrated subsystems for all optical high speed networks,” in Electrochemical Society 18th Meeting, Invited paper, Reno, Nevada, May 1995.
130. H. J. Chao and D. Jeong, “Architecture design of a generalized priority queue manager for ATM switches,” in Intl. Switching Symposium, Germany, Apr. 1995.
131. H. J. Chao and H. Cheng, “A new QoS-guaranteed cell discarding strategy: Self-Calibrating Pushout,” in IEEE Globecom, San Francisco, CA, Nov. 1994.
132. F. S. Choa and H. J. Chao, “A WDM implementation of optically transparent photonic ATM switches, " in IEEE LEOS Annual Meeting, Boston, MA, Nov. 1994.
133. H. J. Chao, “A simple QoS-guaranteed queue management for ATM switches,” invited to The fifth annual TRIO Seminar on Future Trends in Fast Packet Switching, Kingston, Canada, Sep.1994.
134. F. S. Choa and H. J. Chao, “Photonic ATM switches for all optical high-speed networks,” presented at Chinese American Academic and Professional Society CAAPS, New York City, Sep. 1994.
135. B. S. Choe and H. J. Chao, “Fault-tolerance of a large-scale multicast output buffered ATM switch,” in IEEE Proc. INFOCOM, Torando, Canada, June 1994.

136. B. S. Choe and H. J. Chao, “Performance analysis of a large-scale multicast output buffered ATM switch,” in IEEE Proc. INFOCOM, Torando, Canada, June 1994.
137. H. J. Chao and I. H. Pekcan, “Queue management with multiple delay and loss priorities for ATM switches,” in IEEE ICC, New Orleans, LA, May 1994.
138. D. Saha, D. Ghosal, H. J. Chao, “A design for implementation of the Internet Protocol on ATM networks,” in IEEE ICC, New Orleans, LA, May 1994.
139. H. J. Chao and B. S. Choe, “A large-scale multicast output buffered ATM switch,” in IEEE Globecom, Huston, TX, Dec. 1993.
140. H. J. Chao and I. H. Pekcan, “Queue management with multiple delay and loss priorities for ATM switches,” invited talk at The Annual Allerton Conference on Communication, Control, and Computing, University of Illinois, Oct. 1993.
141. H. J. Chao and I. H. Pekcan, “Priority cell departing and discarding in ATM switch nodes,” in IEEE Workshop on High-Performance Communication Subsystems, Williamsburg, Virginia, Sep. 1993.
142. H. J. Chao and N. Uzun, “An ATM queue manager with multiple delay and loss priorities,” in IEEE Globecom, Orlando, FL, Dec. 1992.
143. H. J. Chao and N. Uzun, “A VLSI Sequencer chip for ATM traffic enforcer and queue manager,” in IEEE Globecom, Orlando, FL, Dec. 1992.
144. D. E. Smith and H. J. Chao, “Sizing a packet reassembly buffer at a host computer in an ATM network,” in Second Bellcore Symposium on Performance Modeling, Livingston, NJ, Nov. 1992.
145. H. J. Chao, “A general architecture for link-layer congestion control in ATM networks,” in Intl. Switching Symposium, Yokohama, Japan, Oct. 1992.
146. H. J. Chao, “Architecture design for regulating and scheduling user's traffic in ATM networks,” in ACM SIGCOMM, Baltimore, MD, Aug. 1992.
147. H. J. Chao and D. E. Smith, “Design of a virtual channel queue in an ATM broadband terminal adaptor,” in IEEE Proc. INFOCOM, Florence, Italy, May 1992.
148. D. E. Smith and H. J. Chao, “Buffer sizing at a host in an ATM network,” in IEEE Proc. INFOCOM, Florence, Italy, May 1992.
149. H. J. Chao, “A novel architecture for queue management in the ATM network,” in IEEE Proc. Globecom, Phoenix, Arizona, Dec. 1991.
150. H. J. Chao, D. T. Kong, N. K. Cheung, M. Arnould, and H. T. Kung, “Transport of gigabit/sec data packets over SONET/ATM networks,” in IEEE Proc. Globecom, Phoenix, Arizona, pp. 968-975, Dec. 1991.
151. H. J. Chao, “Design of leaky bucket access control schemes in ATM networks,” in IEEE Proc. ICC, Denver, CO, pp. 180-187, June 1991.
152. C. A. Johnston and H. J. Chao, “Implementation of an ATM layer chip for B-ISDN applications,” IEEE Proc. ICC, Denver, CO, June 1991.
153. H. J. Chao, “Design of a distributed modular Terabit/sec ATM switch,” in IEEE Proc. Globecom, San Diego, CA, Dec.1990.
154. G. Shtirmer and H. J. Chao, “RSTP: a media access control protocol for a broadband customer premises,” in First Bellcore Symposium on Performance Modeling, Livingston, NJ, May 1990.
155. H. J. Chao, G. Shtirmer, and L. S. Smoot, “Design of a SONET/ATM-based optical customer premises network,” in IEEE Proc. Globecom, Dallas Texas, Nov. 1989.
156. H. J. Chao and C. A. Johnston, “A packet video system using the dynamic time division multiplexing technique,” in IEEE Proc. Globecom, Hollywood, Florida, Nov. 1988.
157. H. J. Chao, C. A. Johnston, and L. S. Smoot, “A packet video/audio system using the asynchronous transfer mode technique,” in Proc. Society of Motion Pictures and Television Engineers, New York, NY, October 1988.

158. H. J. Chao and C. A. Johnston, “A packet video system using the dynamic time division multiplexing technique,” in Proc. International Workshop on Packet Video, Torino, Italy, September 1988.
159. H. J. Chao, “Design architectures of a DTDM packet assembler and packet multiplexer,” in IEEE Proc. MONTECH, Montreal, Canada, Nov. 1987.
160. H. J. Chao, T. J. Robe and L. S. Smoot, “A CMOS VLSI framer chip for a broadband ISDN local access system,” in IEEE Symposium on VLSI Circuits, Karuizawa, Japan, May 1987.