Multi-Protocol Label Switching (MPLS)

Multi-Protocol Label Switching (MPLS) is one of the most critical high-speed networking technologies. It is IP-compatible, provides quality of service (QoS) guarantee, and supports high-performance failure recovery. Combining intelligence, scalability, reliability and manageability together, MPLS enables the convergence of multiple protocols (such as IP, Ethernet, ATM, frame relay) to the same backbone network. It is also the key technology to build scalable virtual private networks (VPNs) to support various applications.

This course will cover the fundamental aspects of MPLS and provides a in-depth study of this key technology. We will introduce the essence of MPLS by understanding the major problems of Ethernet switching and IP routing. We will then explain the MPLS architecture and understand the components, including label switching routers, routing, labels, label distribution, and label-switched path. After that we will gain insights into MPLS by discussing its major applications: How to achieve network resilience? How to build VPNs? How to perform traffic engineering? How to guarantee QoS? Throughout the course we will motivate thinking and interactions using various approaches, such as examples, animations, quizzes, and other interactive activities.

CURRICULUM

Module: Fundamentals of Communication Networks
Participants will be able to:
Understand concepts of digital communication, Circuit switching, Packet switching, TDM and SONET Communication Protocols, Ethernet, IP, TCP, UDP and applications, Routing

Module: The Evolution to MPLS
Participants will be able to:
Explore IP Routing, ATM Switching, MPLS, Ethernet Switching, Comparison: Ethernet, IP, and MPLS.
CURRICULUM (continued)

Module: The MPLS Architecture  
*Participants will be able to:*  
Learn Label Allocation, Next Hop Label Forwarding Entry, Label-Switched Path (LSP), Explicit Routing Label Stacking.

Module: Label Switching Routers (LSRs)  
*Participants will be able to:*  
Clearly leverage the Basics of packet switch, Table lookup (MAC table, IP table and MPLS label table), LSR.

Module: MPLS Labels  
*Participants will be able to:*  

Module: Network Resilience  
*Participants will be able to:*  
Learn Requirements on Resilience, Path-based Protection in MPLS, Link-based Protection in MPLS, Failure recovery in IP networks

Module: Virtual Private Networks  
*Participants will be able to:*  
Get an overview of VPNs, Connection-Oriented VPNs, Connectionless VPNs, Comparison of VPN Technologies, MPLS VPN, Advantages of MPLS VPNs, Carrier Ethernet and MPLS VPN.

Module: MPLS Traffic Engineering  
*Participants will be able to:*  
Explore the need for Traffic Engineering on the Internet, Unequal-Cost Load Balancing via Metric Manipulation, MPLS Traffic Engineering Elements (Dynamic/Static LSPs) and MPLS Traffic Engineering Configuration.

Module: MPLS Quality of Service  
*Participants will be able to:*  
Learn introduction to Quality of Service, Integrated Services, Differentiated Services and MPLS QoS Implementation.
Instructor H. Jonathan Chao

Prof Chao, Department Head and Professor of Electrical and Computer Engineering at Polytechnic Institute of New York University, is one of the world’s leading authorities on MPLS. His research is in terabit switches/routers, network security, network on the chip, and quality of service control in high-speed networks. Prof. Chao holds 28 patents with 17 pending and has published more than 180 journal and conference papers. He has also served as a consultant for various companies, such as Huawei, Lucent, NEC, and Telcordia.

Dr. Chao was Co-Founder and CTO of Coree Networks, where he led a team to implement a multi-terabit MPLS switch router with carrier-class reliability. He has been an instructor at University of California at Berkeley and Oxford University’s industry short course programs on SONET, ATM, IP, MPLS, switch/router designs. A Member of Technical Staff at Telcordia, he was involved in transport and switching system architecture designs and ASIC implementations, such as the world’s first SONET-like Framer chip, ATM Layer chip, Sequencer chip (the first chip handling packet scheduling), and ATM switch chip. Dr. Chao was also a Senior Engineer at Telecommunication Labs of Taiwan performing circuit designs for a digital telephone switching system.

Prof. Chao is a Fellow of the IEEE for his contributions to the architecture and application of VLSI circuits in high-speed packet networks. He received the Telcordia Excellence Award in 1987. Co-recipient of the 2001 Best Paper Award from the IEEE Transaction on Circuits and Systems for Video Technology, also co-authored three networking books, Broadband Packet Switching Technologies–A Practical Guide to ATM Switches and IP Routers (Wiley, 2001), Quality of Service Control in High-Speed Networks (Wiley, 2001), and High-Performance Switches and Routers (Wiley, 2007). He has served as a Guest Editor for the IEEE Journal On Selected Areas in Communications (JSAC) on special topics, including “Advances in ATM switching systems for B-ISDN,” “Next generation IP switches and routers,” two issues on “High-performance optical/electronic switches/routers for high-speed Internet,” and “High-speed network security.” He also served as an Editor of IEEE/ACM Transactions on Networking. Prof. Chao received his B.S. and M.S. degrees in electrical engineering from National Chao Tung University, Taiwan and his Ph.D. in electrical engineering from Ohio State University.